RapidCharge™ AC/DC Primary-Side Digital ZVS Flyback Controller

1 Description

The iW9802 is a high-performance AC/DC primary-side digital flyback controller with advanced zero voltage switching (ZVS) and adaptive multi-mode-control (MMC) working with secondary-side regulation (SSR) for applications requiring high power density and high resolution in output voltage/current setting. The device can support rapid charge applications such as travel adapters (TA) of 40W and above. It operates under multi-mode control (MMC) including PWM, PFM and burst mode with main switch ZVS turn-on at high line voltage to achieve less switching loss and low EMI. It also provides a number of key built-in protection features. The iW9802 is optimized to work with Dialog's secondary-side controller, the iW72x, for SSR, synchronous rectifier (SR) control and D+/D- based protocols support. The iW9802/iW72x chipset can achieve tight multi-level constant voltage (CV) and multi-level constant current (CC) regulation in very fine steps for rapid charge applications. With SSR digital compensation, the chipset eliminates the need for external loop compensation components while maintaining stability under all operating conditions.

The iW9802 and iW72x chipset can support D+/D- based protocols to achieve fast and smooth CV/CC transitions upon request by mobile devices (MD). The iW9802 and iW72x chipset can meet no-load power consumption of less than 60mW for typical 40W to 66W designs at 5V output setting.

Dialog's innovative proprietary technology ensures that power supplies designed with the iW9802 and iW72x chipset can achieve high efficiency, high accuracy voltage/current control and fast dynamic load response.

2 Features

- Supports Rapid Charge adapters applications of around 40W and above
- Supports constant-voltage (CV) and constant-current (CC) regulation in fine steps by secondary-side regulation (SSR)
- Dialog's patented adaptive ZVS control minimizes switching loss to enable high efficiency and low EMI
- User configurable ZVS timing to optimize performance for different power MOSFETs
- Adaptive multi-mode control (MMC) using PWM/PFM/Burst modes based on input voltage and output voltage/current improves efficiency across any load and eliminates audible noise
- Adaptive quasi-resonant (QR) mode and continuous conduction mode (CCM) operation at low line voltage
- Built-in single-point fault protections
  - AC line voltage brown-out
  - Output short-circuit
  - Output over-voltage
  - Optocoupler failure
- User programable internal over-temperature protection (OTP) threshold for various thermal requirements
- 10-lead SOIC package

3 Applications

- Rapid-charging AC/DC adapters for smart phones, tablets and other portable devices

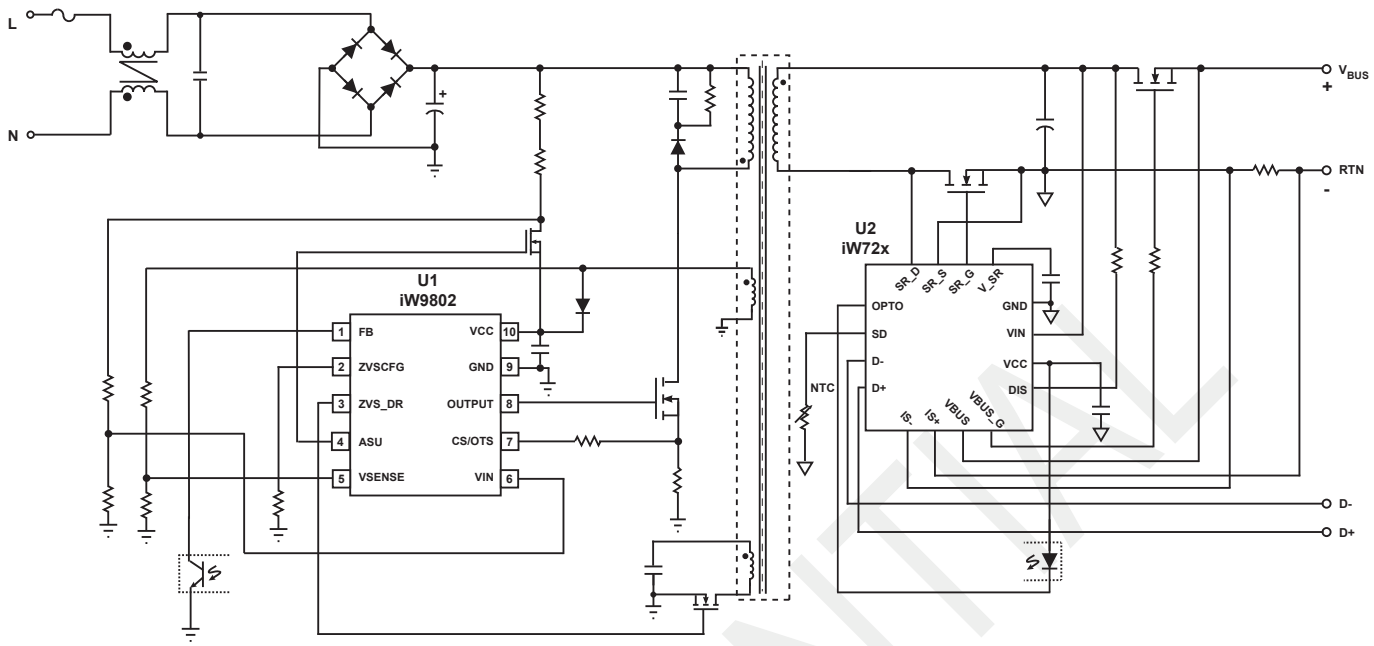


Figure 3.1 : iW9802 Typical Application Circuit with Active Start-up Circuit (Using iW72x as Secondary-Side Controller. Achieving Multi-Level CV/CC Regulation)

4 Pinout Description

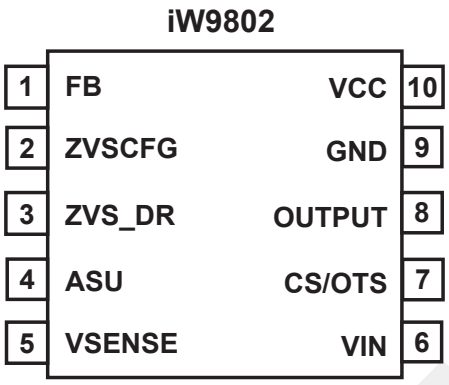


Figure 4.1 : 10-Lead SOIC Package

Pin Number	Pin Name	Type	Pin Description
1	FB	Analog Input	Feedback signal. Used for determining multi-mode control and cycle-by-cycle peak current control.
2	ZVSCFG	Analog Input	ZVS timing configuraton. Used for fine-tuning of ZVS switch ON time.
3	ZVS_DR	Analog Output	Gate drive for auxiliary MOSFET for ZVS purpose.
4	ASU	Analog Output	Control Signal. Used for active start-up device (BJT or depletion mode N-FET)
5	VSENSE	Analog Intput	Voltage sensing. Used for output voltage sensing and auxiliary winding ringing voltage sensing.
6	VIN	Analog Intput	Input AC line voltage detection. Used for AC line voltage detection and optional AC unplug detection for X-capacitor discharge.
7	CS/OTS	Analog Input	Current sensing and over temperature setting. Used for cycle-by-cycle peak-current control and limit. During configuration stage, it can be used to configure certain parameters, such as internal over-temperature protection setting.
8	OUTPUT	Analog Output	Gate drive for power MOSFET.
9	GND	Ground	Ground.
10	VCC	Power Input	IC power supply.

5 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded.

Parameter	Symbol	Value	Units
DC supply voltage range	V_{VCC}	-0.3 to 45	V
Continuous DC supply current at VCC pin (V_{VCC} = 15V)	I_{VCC}	20	mA
VSENSE input (I_{VSENSE} ≤ 10mA)		-0.7 to 10	V
FB voltage		-0.3 to 5.0	V
ZVSCFG voltage		-0.3 to 5.5	V
ZVS_DR voltage		-0.3 to 20	V
VIN voltage		-0.3 to 5	V
ASU voltage		-0.3 to 45	V
CS/OTS voltage		-0.3 to 5.5	V
OUTPUT voltage		-0.3 to 20	V
Maximum junction temperature	T_{JMAX}	150	°C
Operating junction temperature	T_{JOPT}	-40 to 150	°C
Storage temperature	T_{STO}	-65 to 150	°C
Thermal Resistance Junction-to-Ambient	θ_{JA}	160	°C/W
ESD rating per JEDEC JS-001-2017		±2,000	V
Latch-up test per JESD78E		±100	mA

Notes:

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6 Electrical Characteristics

V_{VCC} = 12V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VSENSE SECTION						
Output OVP threshold during normal operation	$V_{VSENSE\_OVP\_OP}$	iW9802-04		3.15		V
		iW9802-16		3.52		
CS/OTS SECTION						
Switching-cycle over-current threshold	V_{OCP1}			0.736		V
CS regulation upper limit (Note 2)	$V_{IPK(HIGH)}$			0.64		V
CS regulation lower limit (Note 2)	$V_{IPK(LOW)}$			0.10		V
OTS configure current source	I_{OTS}			500		µA
FB SECTION						
FB pin internal pull-up resistance	R_{FB}			22		kΩ
FB pin internal voltage source	V_{FB}			4.3		V
OUTPUT SECTION						
Driver pull-down ON-resistance	$R_{DS(ON)\_PD}$	I_{SINK} = 5mA		11.7		Ω
Driver pull-up ON-resistance	$R_{DS(ON)\_PU}$	I_{SOURCE} = 5mA		60		Ω
Rise time (Note 2)	t_{R_OUTPUT}	T_A = 25°C, CL = 330pF, 10% to 90%		95		ns
Fall time (Note 2)	t_{F_OUTPUT}	T_A = 25°C, CL = 330pF, 90% to 10%		14		ns
Output driver voltage source (Note 2)	V_{DR_SOURCE}	V_{VCC} ≥ 12.5V		10.5		V
VCC SECTION						
Operating voltage (Note 2)	V_{VCC}				43	V
Start-up threshold	$V_{VCC(ST)}$	V_{VCC} rising		20		V
Under-voltage lockout threshold	$V_{VCC(UVL)}$	V_{VCC} falling		7	7.5	V
Start-up current	$I_{IN(ST)}$	V_{VCC} = 12V			4	µA
Quiescent current	I_{CCQ}	CL = 330pF, V_{SENSE} = 1.5V		2.75		mA
No-load operating current (Note 2)	I_{CC_NL}	No-load operation		0.6		mA
ASU SECTION						
Resistance between VCC and ASU pin	R_{VCC_ASU}			750		kΩ

Electrical Characteristics (cont.)

V_{VCC} = 12V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ZVS_DR SECTION						
ZVS auxiliary switch driver pull-down ON-resistance	$R_{DS(ON)\_PD\_ZVSDR}$	I_{SINK} = 5mA		12.7		Ω
ZVS auxiliary switch driver pull-up ON-resistance	$R_{DS(ON)\_PU\_ZVSDR}$	I_{SOURCE} = 5mA		30		Ω
Rise time (Note 2)	$t_{R\_ZVS\_DR}$	T_A = 25°C, C_L = 330pF, 10% to 90%		95		ns
Fall time (Note 2)	$t_{F\_ZVS\_DR}$	T_A = 25°C, C_L = 330pF, 90% to 10%		14		ns
ZVS_DR driver voltage source (Note 2)	V_{ZVSDR_SOURCE}			10.5		V
ZVSCFG SECTION						
ZVSCFG current source	I_{ZVSCFG}			500		µA
VIN SECTION						
Brown-in voltage threshold	V_{BROWN_IN}			0.50		V
Brown-out voltage threshold	V_{BROWN_OUT}			0.45		V

Notes:

Note 1. This parameter is not a physical circuit parameter and is for application reference only to set V_{VSENSE} voltage divider resistors.

Note 2. These parameters are not 100% tested. They are guaranteed by design and characterization.

Note 3. Operating frequency varies based on the load conditions, V_{VSENSE} ringing and frequency dithering.

7 Typical Performance Characteristics

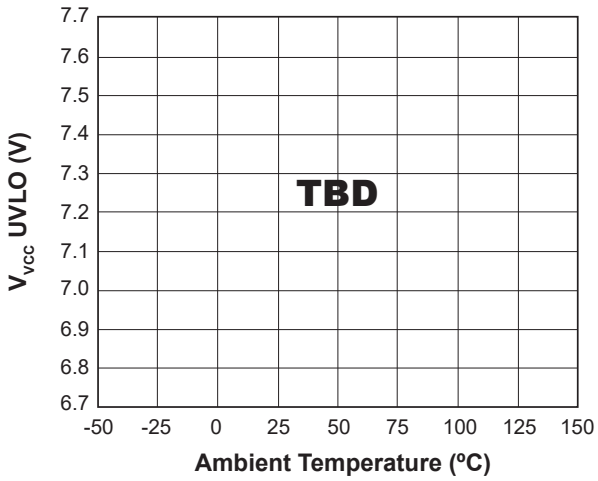


Figure 7.1 : V_{VCC} UVLO vs. Temperature

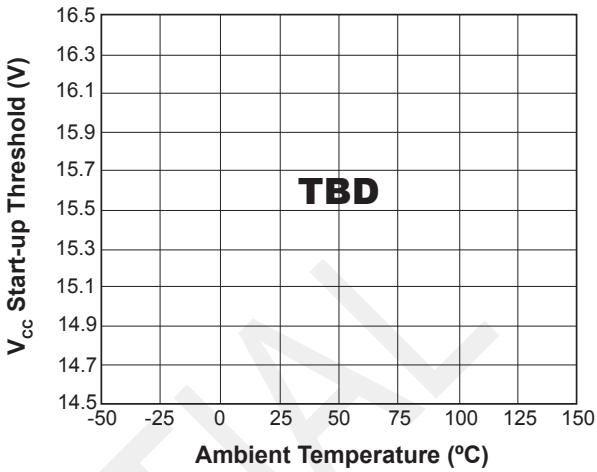


Figure 7.2 : Start-Up Threshold vs. Temperature

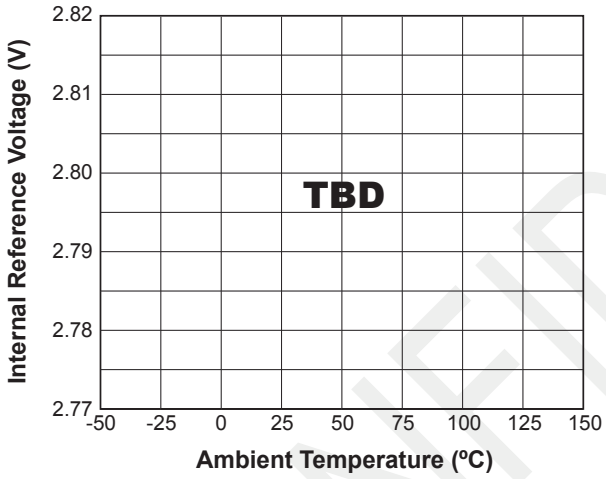


Figure 7.3 : Internal Reference vs. Temperature

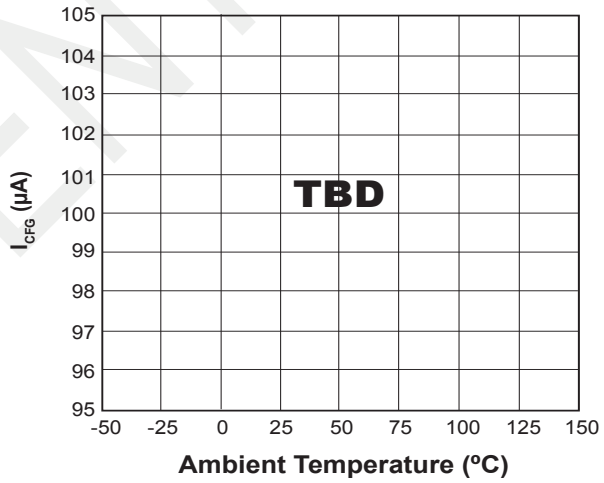


Figure 7.4 : I_{CFG} vs. Temperature

8 Functional Block Diagram

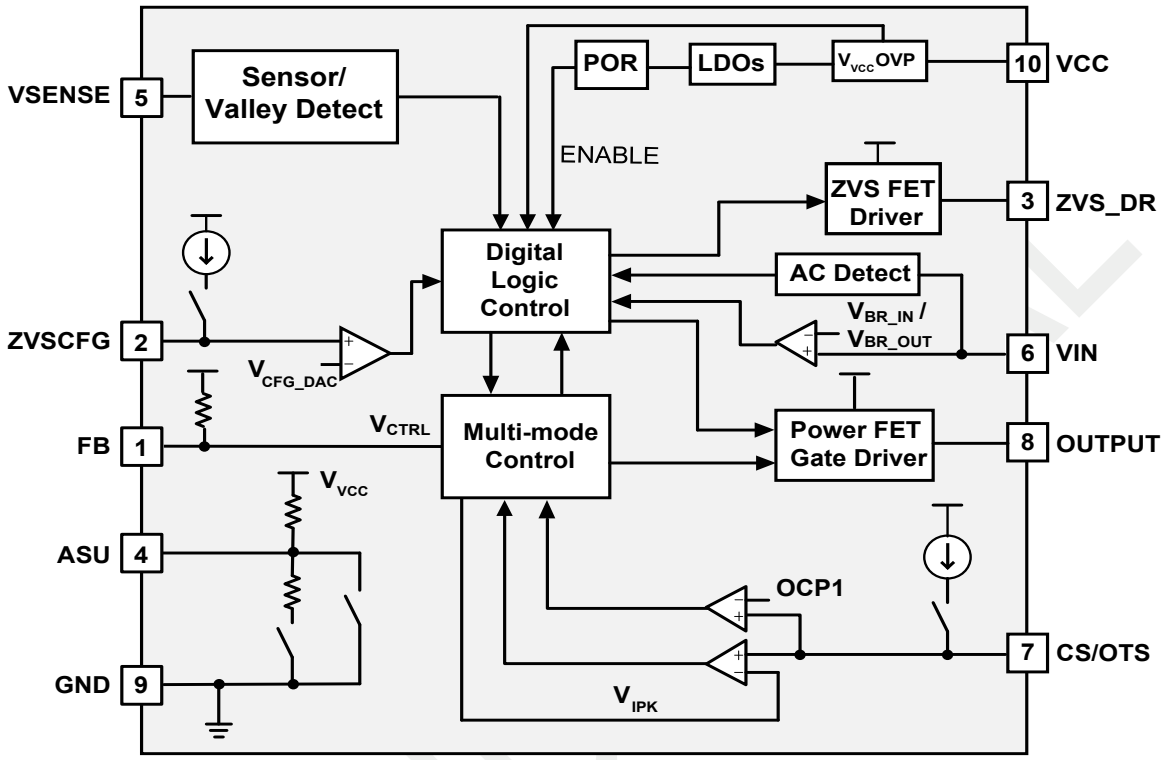


Figure 8.1 : iW9802 Functional Block Diagram

9 Theory of Operation

The iW9802 is an AC/DC primary-side flyback controller with zero voltage switching (ZVS) and multi-mode-control (MMC) working with secondary-side regulation (SSR) for applications requiring high power density and high resolution in voltage/current steps. The iW9802 is optimized to work with the iW72x, Dialog's secondary-side controller, for secondary-side regulation (SSR), synchronous rectifier (SR) control and D+/D- based protocols, to achieve fast and smooth voltage and current transitions upon request from mobile devices (MD). When pairing with the iW72x, the iW9802 can achieve tight multi-level constant voltage (CV) and multi-level constant current (CC) regulation. The chipset eliminates the need for external loop compensation components while maintaining stability over the entire operating range.

Figure 8.1 shows the iW9802 operates in peak current mode control. The multi-mode-control (MMC) block and the digital control logic block generate the multi-mode operation, switching on-time and switching off-time information based on the control signal V_{CTRL} from the FB pin and provide commands to dynamically control the gate voltage of the external MOSFET. The FB pin is used to receive SSR control signal through an optocoupler. The CS/OTS pin is an analog input configured to sense the primary current after internal OTP setting configuration is finished. In order to achieve cycle-by-cycle peak current control and limit, the V_{IPK} signal determined by MMC sets the threshold for the CS/OTS pin voltage to compare with and it varies in the range of $V_{IPK(LOW)}$ to $V_{IPK(HIGH)}$ under different line and load conditions. The ZVS_DR pin is used to drive ZVS auxiliary switch to create ZVS condition for main switch turn-on. The ZVSCFG is for fine-tuning of ZVS auxiliary switch ON time duration. The system loop is compensated by a digital error amplifier in the secondary-side controller, the iW72x. Adequate system phase margin and gain margin are guaranteed by design and no external analog components are required for loop compensation.

The iW9802 uses adaptive multi-mode PWM/PFM/burst mode control to dynamically change the MOSFET switching frequency and V_{IPK} for efficiency, EMI, and power consumption optimization. The built-in single-point fault protection include over-voltage protection (OVP), output short-circuit (SCP), over-current protection (OCP), and current sense fault detection.

Dialog's digital control scheme and patented adaptive ZVS technology are specifically designed to address the challenge and trade-offs of power conversion design. The innovative technologies are ideal for balancing new regulatory requirements for green mode operation with more practical design considerations such as high power density, low standby power and high performance output control.

9.1 Pin Detail

Pin 1 – FB
Feedback voltage signal. It is used for determining multi-mode control and cycle-by-cycle peak current control.

Pin 2 – ZVSCFG
ZVS timing configuration. It is used to fine-tune ZVS switch ON time.

Pin 3 – ZVS_DR
Gate drive for ZVS auxiliary switch.

Pin 4 – ASU
Active startup. It is the control signal for active start-up device (depletion mode NFET).

Pin 5 – VSENSE
Voltage sensing. It is used for output voltage sensing and auxiliary winding ringing voltage sensing.

Pin 6 – VIN
Input Voltage. It is used for input voltage sensing.

Pin 7 – CS/OTS
Current sensing. It is used for cycle-by-cycle peak-current control and limit. During configuration stage, it can be used to configure internal OTP setting.

Pin 8 – OUTPUT
Gate drive for the main switch.

Pin 9 – GND
Ground.

Pin 10 – VCC
Power supply for the controller during normal operation. The controller starts up when the V_{VCC} voltage reaches 20V (typical) and shuts down when the V_{VCC} voltage drops below 7V (typical).

9.2 Active Startup and Soft-Start

The active start-up circuit uses an external depletion mode NFET. Prior to start-up, the ENABLE signal is low and the ASU pin voltage closely follows the VCC pin voltage. Consequently, the depletion mode NFET is switched on, allowing the start-up current to charge the VCC bypass capacitor. When the VCC bypass capacitor is charged to a voltage higher than the start-up threshold $V_{VCC(ST)}$, the ENABLE signal becomes active to turn off depletion mode NFET. The iW9802 begins to perform internal OTP configuration and internal OTP check. Afterwards, the iW9802 commences the soft-start function.

During this start-up process an adaptive soft-start control algorithm is applied, where the initial output pulses are small and gradually get larger until the full pulse width is achieved. The peak current is limited cycle-by-cycle by the V_{IPK} comparator. If at any time the V_{VCC} voltage drops below the under-voltage lockout (UVLO) threshold $V_{VCC(UVL)}$ then the iW9802 goes to shutdown. At this time the ENABLE signal becomes low and the VCC capacitor begins to charge up again towards the start-up threshold to initiate a new soft-start process.

9.3 Working with Dialog's Secondary-Side Controller

The iW9802 works with Dialog's secondary-side controllers, the iW72x family, for SSR, SR control and D+/D- based protocol. An AC/DC power supply designed with the iW9802 and iW72x starts up initially at a default 5V state. During the iW9802 soft-start process, the power supply output voltage ramps up and reaches V_{VIN_POR} of the iW72x at around 3.14V. The iW72x starts initialization and handshaking with iW9802 while iW9802 monitors the opto-coupler current signal through the FB pin. The optocoupler driver current is adjusted adaptively to achieve a smooth ramping until the output voltage reaches 5V, and the iW9802 works with iW72x for SSR-based multi-level CV/CC regulation. iW72x keeps sensing the output voltage and current, which are compared with CV/CC references determined by the D+/D- based protocol. The digital compensator in iW72x generates the control signal for optocoupler driver and optocoupler driver converts the control signal to a proper level of current to drive the diode side of the optocoupler.

The iW9802 receives the secondary side control signal in the format of opto-transistor current through the FB in. The internal control signal for iW9802's multi-mode control is determined by:

$$V_{CTRL} = V_{FB} - I_{OPTO} \times R_{FB} \qquad (9.1)$$

The overall control system including primary side and secondary side is illustrated in Figure 9.1. Dialog's proprietary digital loop compensation and adaptive optocoupler driver and receiver ensure the stable system operation with sufficient margin over wide range of input, output and optocoupler conditions.

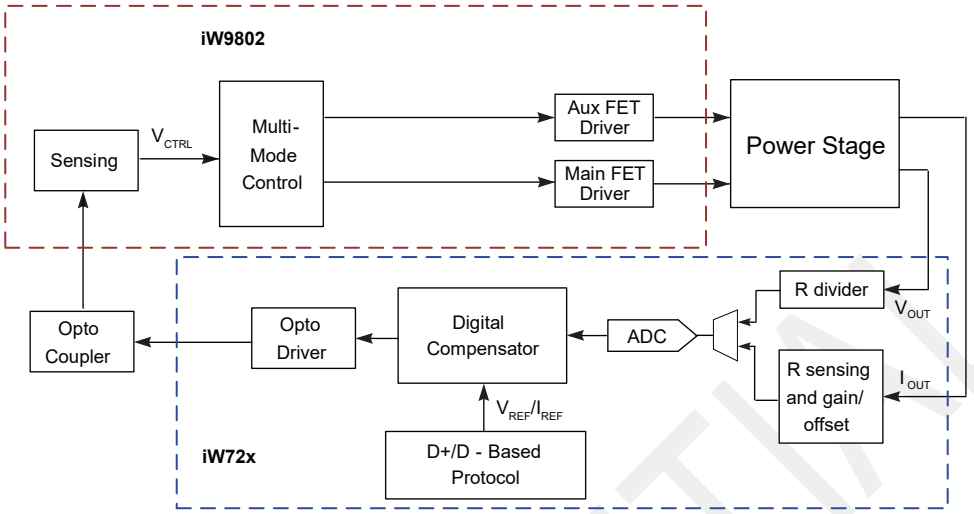


Figure 9.1 : Overall System Level Control with Primary Side and Secondary Side.

9.4 Multi-mode PWM/PFM/Burst Mode Control and Quasi-Resonant Switching

The iW9802 uses a patented adaptive multi-mode control (MMC) with PWM/PFM/burst modes based on the input voltage and output voltage/current to optimize the efficiency and standby power consumption at various load conditions and eliminate audible noise.

During the CV operation and a part of CC operation, the iW9802 normally operates in a pulse-width-modulation (PWM) mode under heavy load conditions. In the PWM mode, the switching frequency keeps around constant while the on-time t_{ON} changes according to the load condition. The maximum switching frequency at PWM mode happens at highest output voltage setting. As the output voltage decreases, the switching frequency at PWM mode decreases accordingly until it reaches 40kHz at 3.3V V_{BUS}.

As the output load decreases, the MMC control adaptively transitions to a pulse-frequency-modulation (PFM) mode. During PFM mode, the power MOSFET is turned on for a set of during under a given instantaneous rectified AC input voltage, but its off time is modulated by the load current. With a decreasing load current, the off-time increases and thus the switching frequency decreases.

When the switching frequency approaches the human ear audible frequency band, the iW9802 transitions to a second level of PWM mode, namely the Deep PWM mode (DPWM). During the DPWM mode, the switching frequency keeps around 25kHz in order to avoid audible noise. As the load current is further reduced, the iW9802 transitions to a burst mode operation to eliminate audible noise. The burst mode keeps the DPWM switching frequency of 25kHz cycle-by-cycle but the switching is enabled/disabled in groups adaptively based on the load condition. The switching group frequency is very low to avoid audible noise frequency range.

The iW9802 also keeps a patented constant-frequency quasi-resonant (QR) switching scheme that has been used in previous generations of Dialog's AC/DC products. Unlike conventional QR modes, this unique QR scheme follows the basic switching frequency profile determined by the MMC control in a deterministic constant-frequency manner, and achieves valley mode turn-on for every PWM/PFM/Burst switching cycle when not running in CCM, during all PWM/PFM/burst modes and in both CV and CC operation. This feature greatly reduces the switching loss and dv/dt across the entire operating range of the power supply.

9.5 Zero Voltage Switching (ZVS)

iW9802 features Dialog patented adaptive zero voltage switching (ZVS) technology to create ZVS condition for main switch turn-on at near zero voltage. This important feature significantly reduces the adaptor switching loss and EMI.
As shown in Fig. 9.2, the ZVS flyback converter controlled by iW9802 is formed based on a conventional flyback converter circuit with the addition of an auxiliary circuit, which consists of a ZVS auxiliary switch, an auxiliary winding and auxiliary capacitor. Depending on the commands generated by the Multi-Mode Control, when it is time to turn on the main switch, the ZVS auxiliary switch is turned on first for a short period of time before the main switch is turned on. During the ZVS auxiliary switch ON time period, the auxiliary capacitor charges the auxiliary winding, and the magnetizing inductance (L_M) current ramps up in the direction opposite to the L_M current in conventional flyback operation. There is primary capacitance (C_P) in the circuit, mainly contributed from the main switch C_{OSS} and transformer interwinding capacitance. After sufficient energy has been built up in L_M, the ZVS auxiliary switch is turned off and a resonance between L_M and C_P starts. During the resonance the voltage across main switch, V_{DS}, decreases to near zero and a ZVS condition for main switch is created. The main switch can then be turned on at ZVS. The primary current is built up, and once it reaches the threshold determined by V_{IPK}, the main switch is turned off, following the peak current mode control.

iW9802 adaptively calculates the ZVS auxiliary switch ON time duration and the time delay from the ZVS auxiliary turn-off instant to the main switch turn-on instant in every switching cycle in accordance with different input and output voltages to create favorable ZVS conditions. This adaptive ZVS timing control is specifically optimized for AC/DC rapid charging applications with wide range of input and output voltage.

Since switching loss is more dominant at high line voltage and conduction loss is more dominant at low line voltage, iW9802 enables ZVS when the adaptor operates at high line voltage and enables quasi-resonant (QR) switching together with CCM at low line voltage.

In order to provide flexibility to fine-tune ZVS auxiliary switch ON time duration during power supply design, a ZVSCFG pin is available the customers so that ZVS auxiliary switch ON time can be configured by an external resistor. Table 9.1 shows the ZVS auxiliary switch ON time offset by ZVSCFG external resistor.

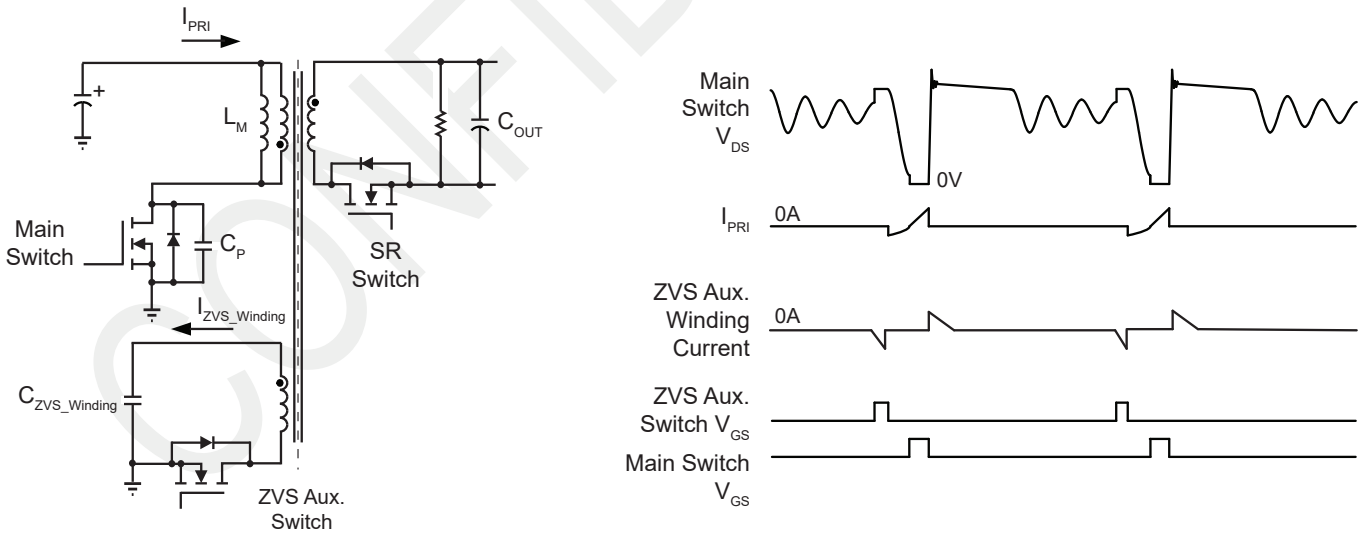


Figure 9.2 : ZVS Operation Circuit and Waveform

ZVSCFG Configuration Resistor Range (kΩ)		ZVS Aux. Switch ON Time Offset (ns)
Min	Max	
5.23	Open	0
4,64	4.87	-300
3.74	3.92	-200
2.87	3.09	-100
2.15	2.43	+100
1.58	1.80	+200
1.10	1.30	+300
0.75	0.887	+400

Table 9.1 Recommended Resistance Range for ZVS Auxiliary Switch ON Time Duration Offset

9.6 Less Than 60mW Standby Power for 40W to 66W Adapter Designs

Under the no-load condition, the iW9802 is operating in burst mode. Although cycle-by-cycle switching frequency is kept at 25kHz, the switching can be disabled by SSR control for a significant long period time at no load condition so that the iW9802 implements an intelligent low-power management technique to achieve ultra-low chip-level operation current when there is no switching event. In addition, the active start-up scheme with depletion mode NFET eliminates the startup resistor power consumption after the ENABLE signal becomes active. When pairing with the secondary-side controller, these features ensure the iW9802 and iW72x chipset can achieve less than 60mW no-load power consumption for typical 40W to 66W adapter designs when the output USB cable is detached and the V_{BUS} voltage stays at 5V.

9.7 Fast Dynamic Load Response

While achieving low standby power, the iW9802 implements proprietary control technology to achieve fast dynamic load response. When a load transient event from light load to heavy load happens, the secondary-side controller iW72x can quickly detect the event, and then responds immediately by increasing the optocoupler driving current and thus increasing the control signal, $V_{CTRL,}$ in the iW9802. Once the iW9802 senses that V_{CTRL} increases, it responses promptly by immediately waking up from low power mode to start switching events, and deliver sufficient power to bring output voltage back to regulation.

9.8 Voltage Protection Features

While the iW72x monitoring output V_{BUS} for overvoltage protection (OVP) and CC shutdown voltage, the iW9802 also implements additional OVP and undervoltage protection. During startup, the iW9802 checks for an OVP fault (typically 6V) before the control handover to the iW72x is completed. After startup, in most conditions, when the output voltage goes beyond the OVP threshold, the iW72x enters fault state and informs the iW9802 to shut down by dramatically reducing optocoupler current. The iW9802 initiates auto-restart after shutdown. The iW9802 also has its additional layer of OVP through the VSENSE pin to provide further protection in some abnormal scenarios.

The iW9802 uses the VIN pin to directly sense the input voltage. It also uses an innovative proprietary digital control method to detect and analyze the switch ON time, which provides real-time indirect sensing and monitoring of the magnitude and shape of the DC bulk capacitor voltage. These enable the iW9802 to determine and distinguish various conditions of the AC input voltage such as brown-out, brown-in, and AC unplug, and to take appropriate actions. When the AC input voltage drops below the normal operation range and the power supply input is still connected to the AC source, the iW9802 initiates a brown-out protection and shuts down the power supply adaptively according

to the power supply load condition. Meanwhile, a brown-in input voltage threshold is set with hysteresis. In the case of the power supply input being unplugged or disconnected from the AC source, the iW9802 continues to control the switching actions to discharge the DC bulk capacitor voltage to a safe level before shutting down the power supply.

Also, the iW9802 monitors the voltage on the VCC pin, and the IC shuts down immediately when the voltage on this pin is below the UVLO threshold. The iW9802 also has a V_{VCC} over-voltage protection (V_{VCC} OVP). During an abnormal event, if the V_{VCC} voltage is higher than the protection threshold, the switching is stopped and the iW9802 shuts down.

When any of these faults are met, the IC remains biased to discharge the V_{VCC} supply voltage. Once the V_{VCC} voltage drops below the UVLO threshold, the iW9802 resets itself and then initiates a new soft-start cycle. The controller continues to attempt a start-up until the fault condition is removed.

9.9 Internal Over Temperature Protection (OTP)

The iW9802 features a configurable internal OTP which shuts down the device if the internal die junction temperature reaches above the internal OTP threshold T_{SD}. The device is kept off until the junction temperature drops below T_{SD-R} (10°C lower than T_{SD}), when the device initiates a new soft-start process to build up the output voltage.

The internal OTP threshold can be configured by connecting a resistor from the CS/OTS pin to the R_{SENSE} resistor. The recommended resistor range and the corresponding internal OTP threshold are listed in the table below. Please note that internal junction temperature may be different to pin temperature and package temperature due to thermal impedance.

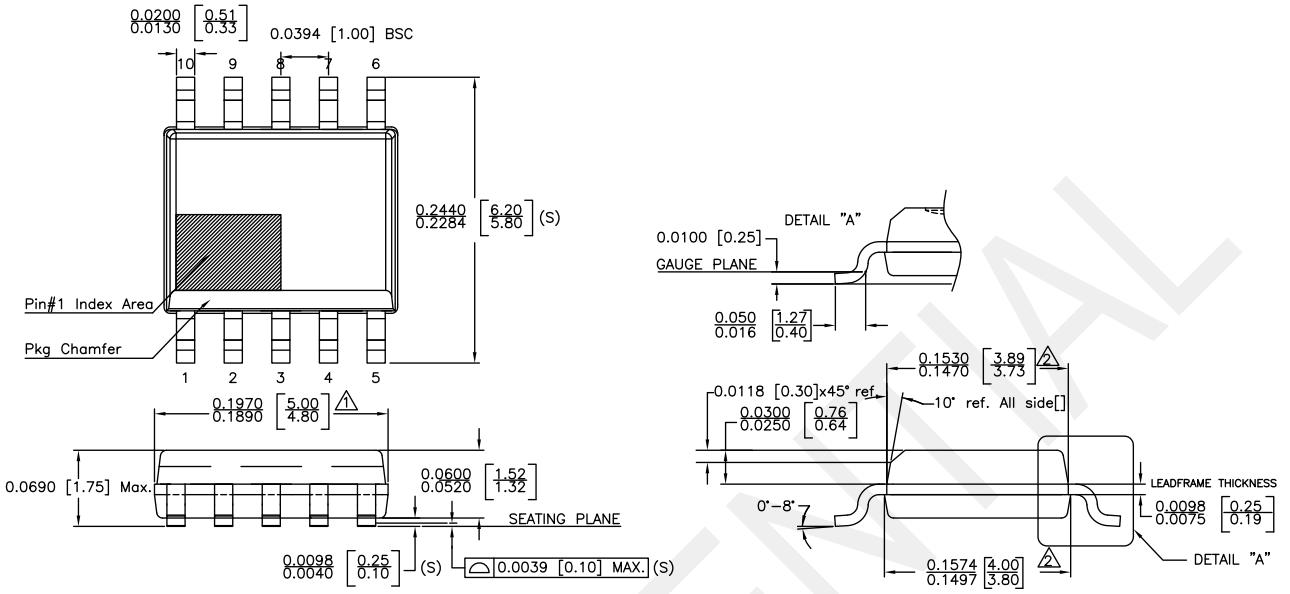
Internal OTP Configuration Resistor Range (kΩ)		Internal OTP Threshold (°C)	
Min	**Max**	**iW9802-04**	**iW9802-16**
3.36	4.10	135	125
2.27	2.67	130	120
1.17	1.76	105	115
0	0.85	100	110

9.10 PCL, OCP and SRS Protection

Peak-current limit (PCL), over-current protection (OCP) and sense-resistor-short protection (SRSP) are features built into the iW9802. With the CS/OTS pin the iW9802 is able to monitor the peak primary current. This allows for cycle-by-cycle peak current control and limit. When the peak primary current multiplied by the current sense resistor is greater than 0.74V, over-current is detected and the IC immediately turns off the gate driver until the next cycle. The output driver sends out a switching pulse in the next cycle, and the switching pulse continues if the OCP threshold is not reached; or, the switching pulse turns off again if the OCP threshold is reached. If the OCP occurs for several consecutive switching cycles, the iW9802 shuts down.

If the current sense resistor is shorted prior to the power supply startup there is a potential danger that over-current condition may not be detected. Thus, the IC is designed to detect this sense-resistor-short fault before start-up and the startup process will not be pursued if the fault exists. The V_{VCC} voltage is discharged since the IC remains biased. Once V_{VCC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting to start up until the fault condition is removed.

10 Physical Dimensions



NOTE :

1. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 INCH PER SIDE.
2. DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 INCH PER SIDE.
3. PACKAGE DIMENSION CONFORM TO JEDEC SPECIFICATION MS–012 EXCEPT LEAD PITCH.
4. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
5. CONTROLLING DIMENSIONS IN INCHES.[mm]
6. PHYSICAL APPEARANCE OF PACKAGE (E–PIN, DIMPLE, CHAMFER) MAY VARY DUE TO ASSEMBLY TOOLINGS

STATUS:	RELEASED
TERMINAL FINISH:	PPF or 100% Sn
TITLE:	SOP 10L 150MIL PACKAGE OUTLINE
REV: C	REVISION NOTE: STANDARDIZED POD

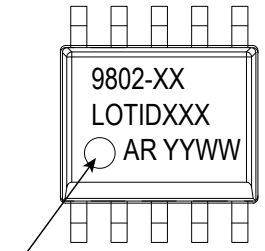
Figure 10.1 : 10-Lead SOIC Package Outline Drawing
(For pin 1 identifier and top marking information, please see section 12)

11 Ordering Information

Part no.	Options							Package	Description
	V_{BUS} range	CCM	ZVS	$F_{SW(MAX)}$ at low line	$F_{SW(MAX)}$ at high line	V_{BUS}/ V_{SENSE}	X-cap discharge		
iW9802-04	3.3V to 12V	Yes	Yes at high line	80kHz	75kHz	5:1	No	SOIC-10	Tape & Reel[1]
iW9802-16	3.3V to 20V	Yes	Yes at high line	90kHz	95kHz	5:0.7	No	SOIC-10	Tape & Reel[1]

Note 1: Tape & Reel packing quantity is 2,500/reel. Minimum packing quantity is 2,500.

12 Top Marking



9802:	iW9802
XX:	Product Option
LOTIDXXX:	Lot Number (can be up to 8 characters)
A:	Assembly Location Code
R:	Product Revision
YY:	Year
WW:	Work Week

Pin 1 marking may vary by assembly supplier, so line 3 left alignment may vary.

Note 1: Font size and text alignment may vary by assembly supplier.

Figure 12.1 : Top Marking for the iW9802

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Contacting Dialog Semiconductor

United Kingdom (Headquarters)
Dialog Semiconductor (UK) LTD
Phone: +44 1793 757700

Germany
Dialog Semiconductor GmbH
Phone: +49 7021 805-0

The Netherlands
Dialog Semiconductor B.V.
Phone: +31 73 640 8822

Email
info_pcbg@diasemi.com

North America
Dialog Semiconductor Inc.
Phone: +1 408 845 8500

Japan
Dialog Semiconductor K. K.
Phone: +81 3 5769 5100

Taiwan
Dialog Semiconductor Taiwan
Phone: +886 281 786 222

Web site:
www.dialog-semiconductor.com

Hong Kong
Dialog Semiconductor Hong Kong
Phone: +852 2607 4271

Korea
Dialog Semiconductor Korea
Phone: +82 2 3469 8200

China (Shenzhen)
Dialog Semiconductor China
Phone: +86 755 2981 3669

China (Shanghai)
Dialog Semiconductor China
Phone: +86 21 5424 9058