AC/DC Secondary-Side Controller with Integrated Synchronous Rectification for USB PD 3.0 w/PPS and Qualcomm® Quick Charge™ 4+ (QC2.0/QC3.0/QC4)

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1 Description

The iW709 is an AC/DC secondary-side controller for USB Power Delivery (PD) 3.0 with Programmable Power Supply (PPS) and Qualcomm® Quick Charge™ QC4+ (QC2.0/QC3.0/QC4) support which integrates a secondary-side regulation controller, interface protocol controller, USB V_{BUS} driver and synchronous rectifier controller into a single IC.

The iW709 allows rapid charge of USB PD PPS or QC-enabled mobile devices (MDs). It resides on the secondary side of an AC/DC travel adapter (TA) and allows the TA to be configured for multi-level output voltage and current.

The iW709 measures the output voltage and load current and sends the results to a digital compensator for closed-loop control of flyback converter. The digital control signal generated by the compensator is converted to an analog signal and transferred to primary controller via an optocoupler.

The iW709 is also an advanced synchronous rectifier (SR) controller with an integrated MOSFET driver. The device works with an external power MOSFET to replace the main rectifying diode on the secondary of a flyback converter. The SR control block optimizes the SR on/off timing and also uses proprietary technologies for timing control of ZVS or active clamp flyback topologies to achieve best efficiency when coupled with Dialog's ZVS-enabled primary-side controllers.

The iW709 can be paired with one of Dialog's high-performance flyback controllers that support either quasi-resonant (QR) control or QR and Zero Voltage Switching (ZVS) technology to achieve high efficiency, low no-load power consumption, accuracy voltage/current control and fast dynamic load response.

2 Features

- USB-IF certified: USB PD 3.0 with PPS
  - » Supports 3.3V to 21V in 20mV steps and output current in 50mA steps
- Optionally supports Qualcomm QC4+ (QC2.0/QC3.0/QC4)
- High resolution accuracy multi-level output voltage and current control
- Built-in digital loop compensation to minimize the external component count
- Built-in synchronous rectification controller with integrated driver
- Optimized V_{DS}-based SR timing and driving control for ZVS or active clamp flyback with wide output range
- NFET driver for V_{BUS} switch
- Programmable active fast discharge from a high voltage to 5V at MD unplug or from a high voltage level to a lower level upon request with built-in switch or external switch
- Intelligent low power mode enables very low no-load power consumption when paired with one of Dialog's primary-side controllers, the iW9801 or iW9809
- Supports DCM and CCM operation
- PD-based power derating feature
- Wide V_{VIN} operating range from 2.6V to 25V
- 16-Lead QFN package

3 Applications

- Direct-charge AC/DC adapters for USB PD enabled smart phones, tablets and other mobile devices

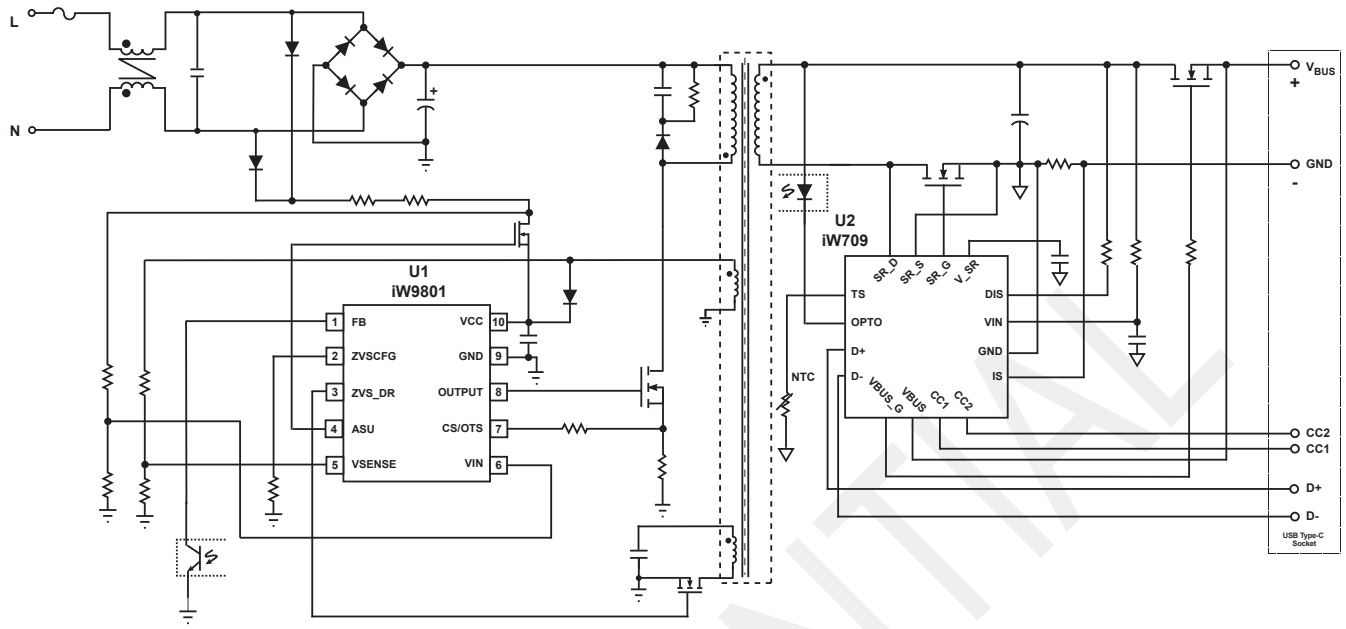


Figure 3.1 : iW709 Typical Application Circuit for Multi-Level Voltage and Current Control with ZVS Technology (Using iW9801 as ZVS-enabled Primary-Side Controller.)

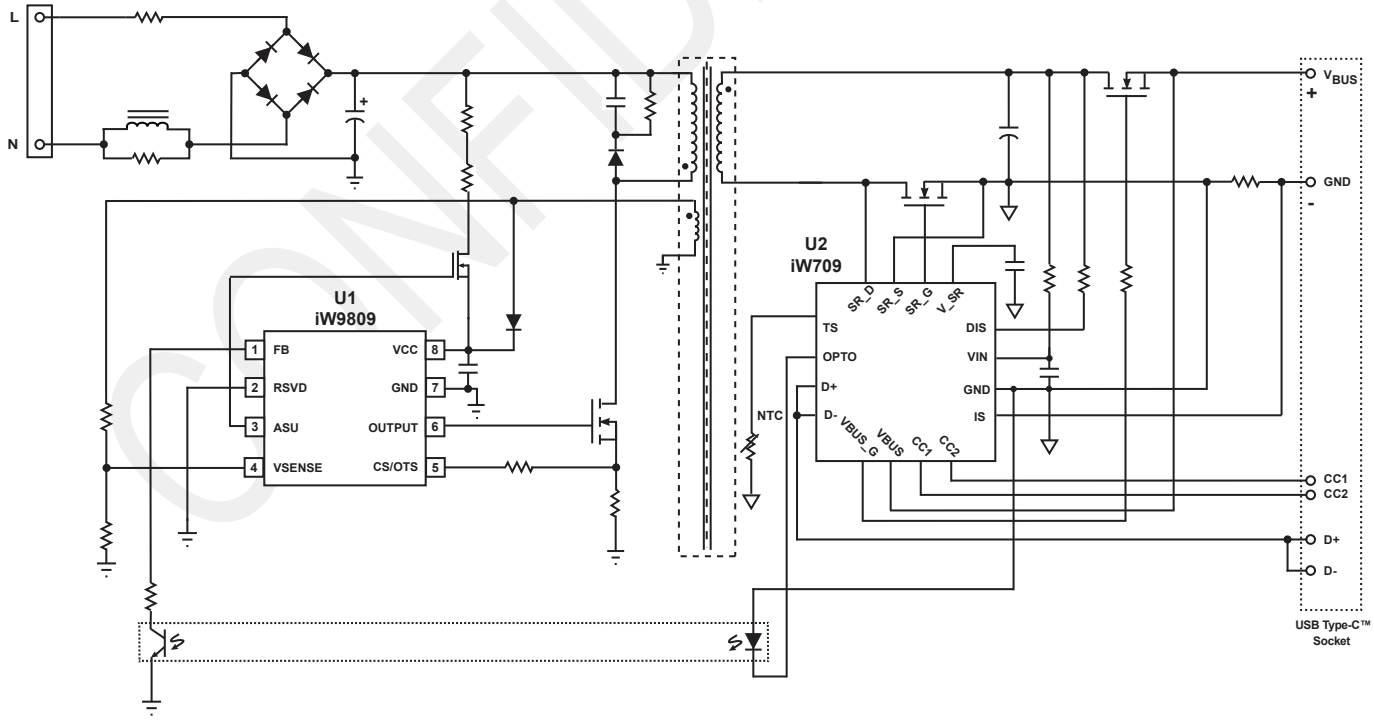


Figure 3.2 : iW709 Typical Application Circuit with Active Start-up Circuit (Using iW9809 as Primary-Side Controller. Achieving Multi-Level CV/CC Regulation and <20mW No-load Power Consumption in a Typical 25W Design)

4 Pinout Description

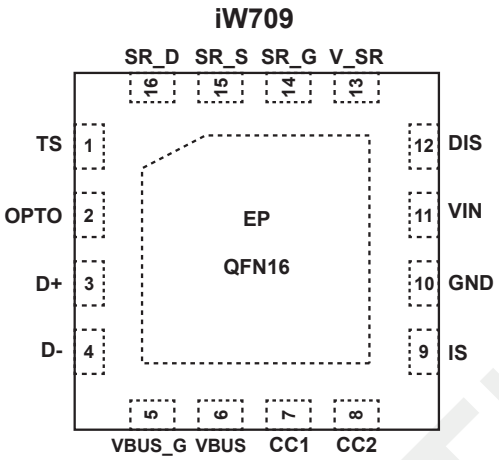


Figure 4.1 : 16-Lead QFN Package

Pin No.	Pin Name	Type	Pin Description
1	TS	Analog Input/ Output	Temperature sensing pin. Connect to an external NTC resistor to measure the power adapter temperature.
2	OPTO	Analog Output	Optocoupler driver to transfer the output regulation control signal to primary side.
3	D+	Analog Input/ Output	USB D+ signal.
4	D-	Analog Input/ Output	USB D- signal.
5	VBUS_G	Analog Input/ Output	Gate drive for external N-FET switch.
6	VBUS	Analog Input/ Output	Connect to V_{BUS} after N-FET switch.
7	CC1	Analog Input/ Output	Communication channel 1.
8	CC2	Analog Input/ Output	Communication channel 2.
9	IS	Analog Input	Output Current sensing , connect to current sensing resistor “+” terminal.
10	GND	Ground	Ground, connect to current resistor “-” terminal.
11	VIN	Power Analog Input	Input of the internal LDO and output voltage sensing circuit.
12	DIS	Analog Output	Discharging circuit. Used for fast discharging of output capacitor.
13	V_SR	Power	Voltage supply for SR drive. Connect this pin to a capacitor.
14	SR_G	Analog Output	Synchronous rectifier MOSFET driver.
15	SR_S	Analog Input	Synchronous rectifier MOSFET source input.
16	SR_D	Analog Input	Synchronous rectifier MOSFET drain voltage sensing and the Pulse Linear Regulator (PLR) input.

5 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to Electrical Characteristics in Section 6.

Parameter	Symbol	Value	Units
V_{VIN} DC supply voltage range (I_{VIN} = 15mA max)	V_{VIN}	-0.3 to 30	V
Continuous DC supply current at VIN pin (V_{VIN} = 12V)	I_{VO}	15	mA
SR_G peak output current	I_G	±2	A
SR_G voltage	V_G	-0.6 to 10	V
SR_D voltage (Note 1)	V_D	-1.5 to 120	V
SR_D peak current	I_{DRAIN}	-40 to 300	mA
SR_S voltage	V_S	-0.5 to 6	V
V_SR voltage	V_{V_SR}	10	V
DIS voltage	V_{DIS}	30	V
Peak current at DIS pin	I_{DIS}	600	mA
OPTO voltage	V_{OPTO}	-0.6 to 30	V
D+ voltage	V_{D+}	-0.3 to 25	V
D- voltage	V_{D-}	-0.3 to 25	V
CC1 voltage	V_{CC1}	-0.3 to 25	V
CC2 voltage	V_{CC2}	-0.3 to 25	V
IS voltage	V_{IS+}	-0.3 to 7	V
TS voltage	V_{SD}	-0.3 to 7	V
VBUS voltage	V_{VBUS}	-0.7 to 30	V
VBUS_G voltage	V_{VBUS_G}	-0.7 to 35	V
Junction temperature	T_J	-40 to 150	°C
Storage temperature		-65 to 150	°C
Thermal Resistance Junction-to-Ambient	θ_{JA}	66.9	°C/W
ESD rating per JEDEC JS-001-2017 (CC1/CC2/D+/D- pins)		± 8,000	V
ESD rating per JEDEC JS-001-2017 (all other pins)		± 2,000	V

Notes:

Note 1. The DRAIN pin voltage should not be below -0.6V for more than 500ns.

6 Electrical Characteristics

V_{VIN} = 5V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{SR} Power Blocks						
Switching between LDO and Pulse Linear Regulator (PLR)						
SR_D operating voltage (Note 1)	V_{SR_D}		-1		100	V
PLR disable threshold at VIN pin	$V_{PLR\_DISABLE}$			6.25		V
PLR enable threshold at VIN pin	V_{PLR_ENABLE}			5.75		V
V_SR LDO						
SR LDO DC regulation voltage	V_{SR_LDO}	V_{VIN} = 8V		6		V
Pulse Linear Regulator (PLR)						
PLR regulation	V_{PLROUT}	I_{LOAD} = 5mA, V_{SR_D} = 10V, 25°C		6		V
VIN Power Blocks						
V_{VIN} POR threshold	V_{VIN_POR}			3.14		V
V_{VIN} UVLO threshold	V_{VIN_UVLO}			2.6		V
V_{VIN} maximum operation voltage (Note 1)	V_{VIN}				25	V
Synchronous Rectifier Blocks						
Gate pull-up resistor	R_{UP}			12		Ω
Gate pull-down resistor	R_{DOWN}			1.6		Ω
Gate output high voltage (Note 1)	V_{G_H}			V_{V_SR} - 0.2		V
Gate output low voltage (Note 1)	V_{G_L}				0.2	V
Gate rising time (Note 1)	t_{G_RISE}	C_G = 4.5nF, V_{VIN} = 5V, 1V to 6V		80		ns
Gate falling time (Note 1)	t_{G_FALL}	C_G = 4.5nF, V_{VIN} = 5V, 6V to 1V		22		ns
SR function enable voltage at V_SR pin	$V_{SR\_EN\_VSR}$			3.35		V
SR function disable voltage at V_SR pin	$V_{SR\_DIS\_VSR}$			3.25		V
SR turn-on threshold	V_{ON_TH}			-120		mV
SR turn-off threshold	V_{OFF_TH}			-3		mV
Ringing detection threshold	V_{RING_TH}			0.4		V
Minimum on time	t_{ON_MIN}			1		µs

6 Electrical Characteristics (continued)

V_{VIN} = 5V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OTP Section						
TS pin sourcing current, high	I_{TS_HIGH}			100		µA
TS pin sourcing current, low	I_{TS_LOW}			5		µA
TS pin NTC temperature - turn-off V_{BUS} switch and shutdown TA (Note 1)	T_{TS_OTP}			120		°C
IC junction temperature - turn-off V_{BUS} switch and shutdown TA (Note 1)	T_{J_OTP}			140		°C
IC junction temperature - turn-on V_{BUS} switch (Note 1)	T_{J_ST}			120		°C
Protocol Blocks						
Discharge/OV Thresholds						
Threshold to end fast discharge (Note 1)	$V_{IN(DIS\_FAST)}$	Minimum clamp to target voltage +160mV		(Target voltage) +1.5		%
Threshold to end slow discharge (Note 1)	$V_{IN(DIS\_SLOW)}$			(Target voltage) +60		mV
Over-voltage threshold (Note 1)	$V_{IN(OV)}$			(Target voltage) +2		V
DIS pin fast discharge internal resistance	R_{FAST}			7	20	Ω
Slow discharge current	I_{SLOW}			30		mA
VBUS SECTION						
VBUS discharge resistor (Note 1)	R_{VBUS_DIS}			10		kΩ
VBUS leakage impedance (Note 1)	R_{VBUS_LKG}	V_{BUS} switch off	72.4			kΩ
VBUS attach/detach detection threshold	V_{SAFE_0V}			0.6		V
VBUS output short detection threshold	V_{OSP}			360		mV
V_{BUS_G} SECTION						
V_{VBUS_G} to V_{VBUS} regulation range	V_{GS}	V_{VIN} = 5V, I_{GATE} = 110µA		6.9		V
V_{VBUS_G} to V_{VBUS} resistor	R_{GS}			2000		kΩ

6 Electrical Characteristics (continued)

V_{VIN} = 5V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ADC SECTION						
V_{VIN} sensing range (Note 1)	V_{VIN_RANGE}		2.8		23.26	V
V_{VIN} sensing tolerance	V_{VIN_TOL}				2	%
IS sensing range (Note 1)	I_{IS_RANGE}		0		6.5	A
IS sensing tolerance	I_{IS_TOL}		-150		150	mA
TS sensing tolerance	TS_{TOL}	T_{NTC} > 60°C	-5		5	°C
Junction temperature range (Note 1)	T_{J_RANGE}		0		150	°C
Junction temperature range tolerance (Note 1)	T_{J_TOL}		-10		10	°C
VCONN SECTION						
VCONN voltage			3		5.5	V
VCONN current	I_{VCONN}	V_{VCONN} = 3V	21			mA
VCONN discharge resistor	R_{DIS_VCONN}			2.6		kΩ
PD/QC MODE TIMING						
Time from attach MD to V_{BUS} reach 5V (Note 1)	T_{BUS_ON}		0		275	ms
Time from detach MD to V_{BUS} below V_{SAFE_0V} (Note 1)	T_{BUS_OFF}		0		650	ms
Error recovery time (Note 1)	$T_{RECOVERY}$			5		s
D+/D- SECTION						
Data detection voltage	V_{DAT_REF}			0.35		V
V_{OUT} selection reference	V_{SEL_REF}			2.05		V
D+ to D- resistance when shorted	R_{DCP_DAT}	D+ = D- = 0.6V		15		Ω
D+ pull-down resistance	R_{DP_DOWN}			1000		kΩ
D+ OVP threshold	V_{DP_OVP}			4.5		V
D- OVP threshold	V_{DM_OVP}			4.5		V
OPTO SECTION						
Maximum OPTO drive current (Note 1)	I_{OPTO_MAX}			1.8		mA

6 Electrical Characteristics (Cont.)

V_{VIN} = 5V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CC1/CC2 SECTION						
CC1 sourcing current (Note 2)	I_{CC1}	Default current limit 2A		180		µA
		Default current limit 3A		330		
CC2 sourcing current (Note 2)	I_{CC2}	Default current limit 2A		180		µA
		Default current limit 3A		330		
MD pull-down resistor R_D detect threshold	V_{TH_RD}			2.9		V
Cable pull-down resistor R_A detect threshold	V_{TH_RA}			0.5		V
CC1 pull-up resistor (detach state) (Note 1)	R_{CC1_DETACH}			56		kΩ
CC1 OVP threshold	V_{CC1_OVP}			5.7		V
CC2 OVP threshold	V_{CC2_OVP}			5.7		V
BMC signal logic high voltage	$V_{CC\_TX\_HIGH}$			1.125		V
BMC signal logic low voltage (Note 1)	$V_{CC\_TX\_LOW}$		-75		75	mV
BMC receiver comparator threshold (rising/falling)	$V_{TH\_CC\_RX}$	Rising		0.725		V
		Falling		0.575		
BMC signal bit rate (Note 1)	f_{BMC}		270	300	330	kbps
BMC transmitter output impedance	Z_{DRIVER}	T_A = 25°C	33		75	Ω

Notes:

Note 1: These parameters are not 100% tested. They are guaranteed by design.

Note 2: Value used depends upon specific product option

Note 3: Parameter can be configured by manufacturer. Please contact Dialog for NTC selection and OTP threshold information.

7 Typical Performance Characteristics

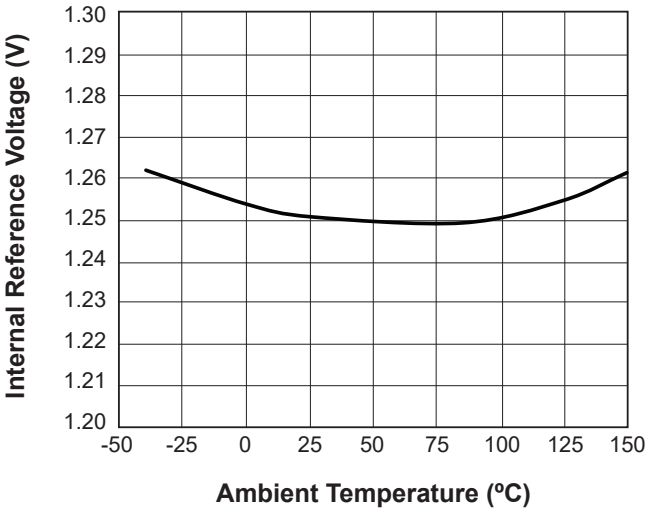


Figure 7.1 : Internal Reference Voltage vs. Ambient Temperature

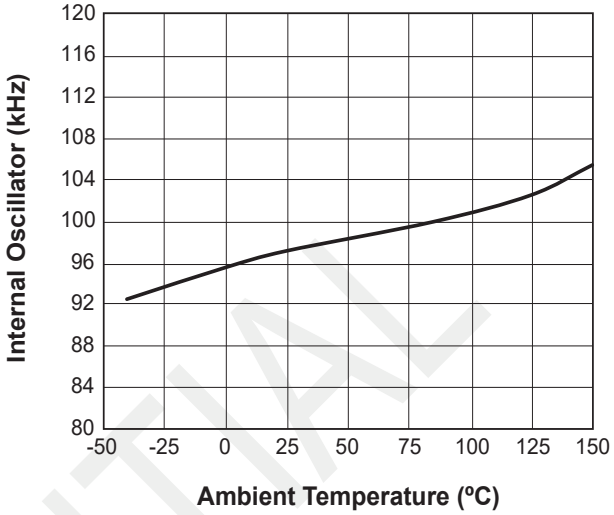


Figure 7.2 : Internal Clock Frequency vs. Ambient Temperature

8 Functional Block Diagram

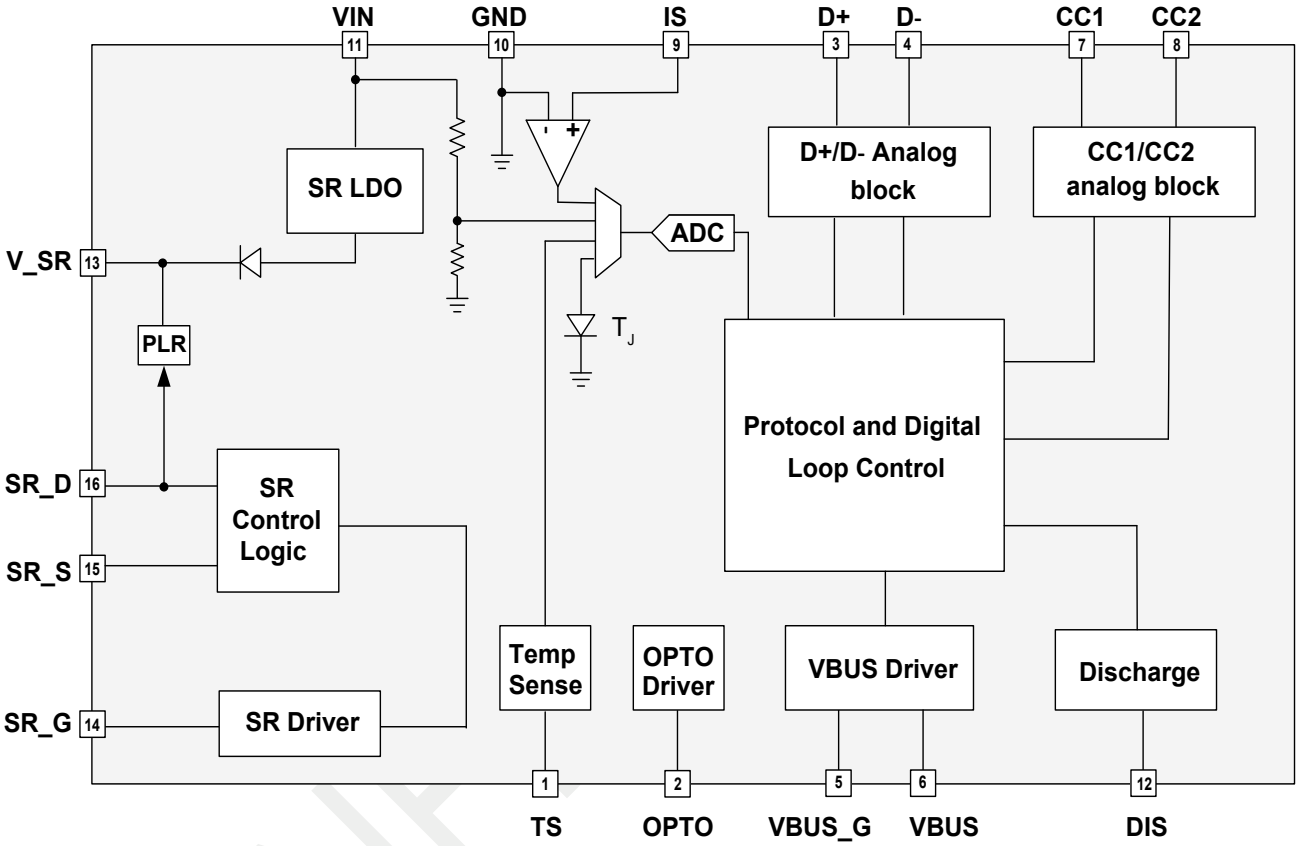


Figure 8.1 : iW709 Functional Block Diagram

9 Theory of Operation

The iW709 is a secondary-side controller for AC/DC adapter. It integrates the synchronous rectifier driving, secondary-side regulation and USB PD 3.0/QC protocols in one IC to provide high-performance and cost-effective rapid charge solutions.

The iW709 can interface with MDs equipped with USB PD 3.0/QC technology. It is also backward compatible with USB BC1.2 compliant MDs and other MDs to provide a 5V output by default setting. The iW709 can be detected as a DCP if an USB PD 3.0/QC-equipped MD is connected. After the initial detection stage, the iW709 interprets the MD based on its CC1/CC2/D+/D- signal voltage to be either an USB PD 3.0/QC device and reads its associated output voltage/current requests. When iW709 receives a valid voltage/current request, it adjusts the voltage/current target of the control loop accordingly to regulate the output voltage/current to the requested level. The iW709 also monitors the TA output voltage and protects the TA under over-voltage or over-current condition. The iW709 also features a programmable active discharging function to discharge the output capacitor in a short time after a request for a lower voltage or unplug of USB PD 3.0/QC-equipped MDs. The iW709 also integrates a 10-bit ADC for accurate output voltage, current and internal/external temperature measurement. The MD can read TA-side V_{BUS} voltage, current and temperature through PD command.

The iW709 features a built-in digital compensator for output voltage/current regulation. It eliminates the need of external compensation resistors and capacitors. The output voltage and current are sampled by the 10-bit ADC and fed into the digital compensator. The digital compensator generates the error signal by comparing the requested voltage/current from the MD to the actual output voltage/current. Based on the error signal the digital compensator further generates an output regulation control signal and feeds to the optocoupler driver. The optocoupler driver converts the output regulation control signal to a driving current at the cathode of the optocoupler input side to send the signal to the primary controller.

The iW709 can be paired with one of Dialog's high-performance primary-side controllers, the iW9801 which supports ZVS solutions and the iW9809, which supports QR solutions, to achieve high efficiency, low no-load power consumption, accuracy voltage/current control and fast dynamic load response.

The iW709 builds in the synchronous rectifier (SR) control function with a MOSFET driver that uses an external power MOSFET to replace the main rectifying diode on the secondary of a flyback converter. It measures the voltage across the synchronous MOSFET to achieve lossless current sensing for the driver timing control. The digital SR logic control block generates the gate driver control signal based on the drain-to-source voltage of the synchronous MOSFET. The gate driver control signal is fed into the integrated MOSFET driver to drive the synchronous MOSFET. The gate driver voltage is regulated for optimum driving efficiency and on/off timing. The iW709, when paired with the iW9801, ZVS-enabled primary-side controller, optimizes the SR on/off timing and driving voltage for ZVS or active clamp flyback by differentiating the switching action of primary main switch and auxiliary switch. The SR MOSFET is only turned on after the main switching turn off. It remains off during auxiliary switch on-time.

9.1 Pin Detail

Pin 1 – TS
Connect to an external NTC resistor to measure temperature.

Pin 2 – OPTO
Optocoupler driver output. It is a current sink controlled by the digital compensator. Connect this pin to the cathode of the optocoupler input diode. The anode of the optocoupler input diode should be connected to the VIN pin through a resistor.

Pin 3 – D+
USB D+ signal.

Pin 4 – D-
USB D- signal.

Pin 5 – VBUS_G
Connect to external N-FET gate pin for V_{BUS} switch gate-source voltage control.

Pin 6 – VBUS
Monitor V_{BUS} voltage. Used for V_{BUS} switch control and output short circuit protection.

Pin 7 – CC1
USB Type-C configuration channel pin 1. Used for MD attach/detach detection and PD communication.

Pin 8 – CC2
USB Type-C configuration channel pin 2. Used for MD attach/detach detection and PD communication.

Pin 9 – IS
Output current sensing resistor + terminal input. See figure 3.1.

Pin 10 – GND

Pin 11 – VIN
Input of the internal LDO and output voltage sensing circuit. Connect the output capacitor of the TA to this pin through an RC filter.

Pin 12 – DIS
Programmable active discharge. This pin provides a discharge path for the external circuit, such as an output capacitor. It can also drive an external P-channel FET. When there is a request for a lower voltage or the USB MD is unplugged at a high voltage, the internal active discharge switches are turned on.
Ground.

Pin 13 – V_SR
Voltage supply for SR drive. Connect this pin to a capacitor. The "-" terminal of the capacitor should connect to the TA output capacitor "-" terminal.

Pin 14 – SR_G
Synchronous rectifier MOSFET driver.

Pin 15 – SR_S
Synchronous rectifier MOSFET source voltage sensing.

Pin 16 – SR_D
Synchronous rectifier MOSFET drain voltage sensing and the Pulse Linear Regulator (PLR) input.

9.2 Initialization and Handshaking with the Primary-Side Controller

An AC/DC power adaptor designed with the iW9801/iW9809 and iW709 starts up initially at a default 5V state. During startup, before the VIN voltage of the iW709 reaches V_{VIN_POR}, the optocoupler driver of the iW709 is turned off. The iW9801/iW9809 controls the TA output voltage ramping independently. As soon as V_{VIN} of iW709 reaches V_{VIN_POR}, the iW709 starts the initialization and monitors the output voltage. The optocoupler driver sink current is adjusted based on output voltage to achieve a smooth ramping until the output voltage reaches 5V. The iW709 turns on the V_{BUS} switch if MD plug_in is detected.

9.3 CC1/CC2 Attach/Detach Detection and V_{BUS} Control

The V_{BUS} switch is off initially upon travel adapter (TA) power up. After the output voltage (and V_{VIN} of iW709) of the TA reaches V_{VIN_POR}, CC1 and CC2 are connected to a voltage source, V_{REG} (about 4.5V), through two 56kΩ resistors (R_{CC1_DETACH}). The CC1 and CC2 voltages are compared with V_{TH_RD} to detect if the mobile device (MD) or cable is attached. The MD or cable attach will cause the CC1 and/or CC2 voltage to be lower than V_{TH_RD}. Once the MD and/or

cable attach is detected, the iW709 will apply I_{CC1} and I_{CC2} on CC1 and CC2 simultaneously to determine if CC1 and CC2 are connected to R_D (5.1kΩ to GND inside MD) or R_A (1kΩ to GND inside cable) by comparing CC1/CC2 voltage with V_{TH_RD} and V_{TH_RA}. The V_{BUS} switch will turn on after 150ms if the following three conditions are met:

1) V_{BUS} is less than V_{SAFE_0V}

2) V_{VIN} is 5V

3) Only one of CC1 and CC2 connects to R_D and the other one connects to R_A or open

After the V_{BUS} switch turns on, the iW709 determines which of the two currents, I_{CC1} or I_{CC2} that was previously applied to CC1 and CC2 respectively, was connected to R_A (or open) and will turn off that current source. The remaining I_{CC1}/ I_{CC2} current will only apply to the CC pin that connects with R_D so that it can detect when the MD detaches. If the MD is detached, the CC1 or CC2 voltage originally connected with R_D will be higher than V_{TH_RD} to indicate the MD is detached. The V_{BUS} switch will thus turn off and V_{BUS} will be discharged through R_{VBUS_DIS} if $V_{BUS}>V_{SAFE\_0V}$. R_{VBUS_DIS} will disconnect after $V_{BUS}<V_{SAFE\_0V}$ or the connect time exceeds 650ms.

At this point, the iW9801/iW9809 and iW709 will change the output voltage (and V_{VIN} of the iW709) to the default 5V level if it is not already 5V. The current limit will be set to the default level per product options. Two 56kΩ resistors (R_{CC_DETACH}) will be reconnected to CC1/CC2 from V_{REG} to start a new attach detection cycle.

9.4 Protocol Initialization and Handshaking

An AC/DC power adapter designed with the iW9801/iW9809 and the iW709 starts up initially at its default 5V output voltage setting. Meanwhile, D+/D- are shorted together by an internal switch to indicate DCP role for BC1.2 detection. When the TA is connected to the MD and V_{BUS} switch is on, the iW709 begins the protocol detection procedure. The iW709 sends out USB PD Source_Capabilities messages via the CC pin (either CC1 or CC2, whichever pin is connected to R_D) and waits for the MD's response in order to make a PD explicit contract. While waiting for a response, the iW709 starts the BC1.2 detection procedure through the D+/D- pins followed by the QC2.0/QC3.0 detection procedure (if QC2.0/QC3.0 is enabled by IC option), also through the D+/D- pins. If the PD protocol is detected first, the QC2.0/QC3.0 protocol is disabled and PD is used until detach. If the QC2.0/QC3.0 protocol is detected first, the iW709 will enter QC2.0/QC3.0 mode and meanwhile continue to send Source_Capabilities and wait for a response from the MD. If PD is not detected after about 7.5 seconds, the iW709 will stop sending Source_Capabilities and stay in QC2.0/QC3.0 mode. If the MD responds and makes a PD explicit contract, the iW709 will exit QC2.0/QC3.0 mode and stay in PD mode until detach. If neither PD nor QC are detected after 7.5 seconds, the TA will disable PD detection and remain in QC detection mode. While the TA is in QC2.0/QC3.0 mode or QC2.0/QC3.0 detection mode, if a PD Hard Reset message is received, the iW709 will disable the V_{BUS} switch for 0.85 seconds and enable the V_{BUS} switch again at the default output voltage of 5V and default current and start the PD and QC2.0/QC3.0 detection procedure again as described previously. Figure 9.2 shows the flowchart for the attach and detection sequence for a travel adapter using the iW709.

9.5 PD Mode Operation

The iW709 integrates a USB PD Biphase Mark Coding (BMC) signal transmitter/receiver and can communicate with the MD directly through the CC1/CC2 pin. It supports both PD2.0 and PD3.0 protocol. The iW709 uses the PD3.0 protocol if the MD is equipped with PD3.0. It will automatically change to use PD2.0 protocol if the MD connected only supports the PD2.0 protocol. The iW709 supports up to 7 Power Data Objects (PDOs). The power negotiation process starts with the iW709 sending it's Source_Capabilities with all the PDOs it supports. The MD evaluates the received PDOs and requests one of the PDOs. If the request is valid, the iW709 changes the output voltage and output current limit to the requested value. The iW709 informs the MD when the TA's voltage and current reach the requested level.

The iW709 also supports direct charge (V_{BUS} connects to the MD battery through a switch instead of through a buck converter) operation with the MD through Programmable Power Supply (PPS) Augmented Power Data Objects

(APDO). The MD can make a contract with the iW709 at the APDO through standard power negotiation process. When the MD and TA are contracted with APDO, the MD can request any voltage within the APDO voltage range in 20mV steps. The MD can also request any TA output current within the APDO current range in 50mA steps. The internal ADC of the iW709 measures V_{BUS}, I_{BUS}, and TA temperature. This information is saved in the iW709's internal registers and can be read by the MD through PD PPS_Status and Status messages.

Some of the USB PD features are not supported by iW709:

- USB Type-C Alternate mode
- USB Type-C Audio Adapter and Debug Accessary mode
- USB PD BFSK communication through V_{BUS}
- USB PD Dynamic Power Capability
- USB PD Peak Current Operation
- USB PD Power Role Swap and Fast role Swap

9.6 VCONN Support and Cable Reading

The USB PD specification supports TA current up to 5A. However, standard USB Type-C™ cables have a maximum current rating of 3A. If the TA has a PDO/APDO current higher than 3A, it needs to ensure that the cable used has a current rating higher than 3A. USB PD requires use of either a captive cable or an Electronically Marked Cable for > 3A applications. The iW709 provides an optional VCONN and cable reading feature to work with EMC. When this feature is enabled, after cable plug in is detected and the TA turns on the output voltage to 5V, the iW709 will connect the VCONN terminal (the CC1 or CC2 terminal that is not used as PD communication channel) to V_{VIN}, which is set to 5V. The VCONN voltage source provides the external power supply to the EMC internal circuit. After the VCONN voltage turns on for 135ms, the iW709 will send a PD Discover_Identity message to the EMC to read the EMC current rating. The iW709 will turn off the internal VCONN switch and start sending out Source_Capabilities after the cable reading. If no response from the cable is received or the cable current rating is 3A, the iW709 will limit its PDO current to 3A maximum. The iW709 will turn on VCONN and cable reading again after plug-in and Hard Reset.

9.7 QC Mode Operation (Optional)

After initialization and handshaking with the MD, if there is a D+/D- combination change and the D+/D- voltage combination is a valid QC2.0/3.0 request and passes the 40ms deglitch filter, the iW709 enters QC2.0/3.0 mode.

The iW709 interprets the D+/D- combination according to the QC2.0/3.0 specification. The interpretation of the D+/D-combination and voltage requests are listed in Table 9.1.
Please note that a voltage at D+ or D- is detected as:

a) 0V, if it is lower than V_{DAT_REF};

b) 0.6V, if it is between V_{DAT_REF} and V_{SEL_REF};

c) 3.3V, if it is higher than V_{SEL_REF}.

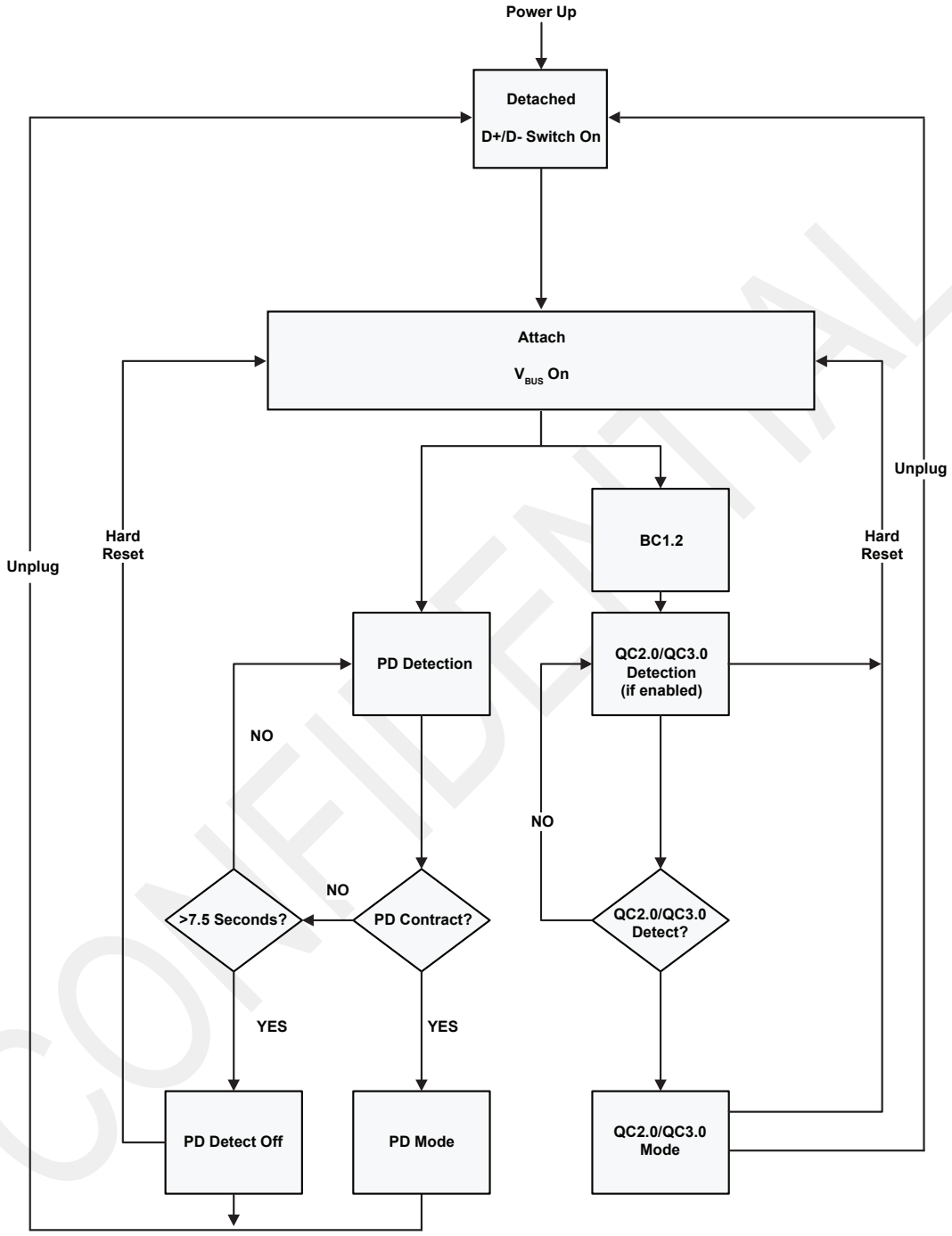


Figure 9.1 : Attach and Detection Flowchart for BC1.2, USB PD 2.0/3.0 and QC2.0/3.0.

D+	D-	V_{OUT}
0.6V	0.6V	12V
3.3V	0.6V	9V
0.6V	3.3V	Enters continuous mode
0.6V	0V	5V
3.3V	3.3V	20V (optional)
All other combinations		Stays unchanged

Table 9.1: D+/D- Signals and Adapter V_{OUT} (aka V_{BUS}, V_{VIN})

9.8 Programmable Active Discharge

Discharge of the output capacitor is necessary for a quick voltage transition from a higher level to a lower level when a lower voltage is requested. An internal switch between the DIS pin and GND pin is turned on to provide a current path from the output voltage through an external resistor to ground. The discharging time is programmable with the external resistor. A resistance of 47Ω or higher is recommended for the external resistor to prevent over-current or over-heating inside the IC.

If the application uses a larger output capacitor or requires faster discharging, an external P-channel FET can be used and the iW709 DIS pin can be used to drive the FET. When the MD is unplugged, the iW709 resets to its initial setting. The active fast discharge starts after a confirmed lower voltage request; it stops when the active discharge threshold of the target voltage is reached or a 200ms timer (including de-glitch time) expires to avoid excess load current and high power dissipation inside the IC. After the active fast discharge stops, a slow discharge path continues to discharge the output capacitor until voltage reaches target for the 200ms timer expires.

9.9 V_{BUS} Switch Output Short Protection

After the MD is attached to a Type-C connector, the iW709 will turn on the V_{BUS} NFET switch after 150ms. If the V_{BUS} switch turns on into an output short, the output capacitor discharge current may exceed the NFET's maximum current limit and damage the NFET. The iW709 implements a soft-start scheme to ensure the output current rises slowly while the output capacitor discharges. The output short is detected when V_{BUS} discharges below a threshold (V_{VIN_LOW}) lower than the normal V_{OUT} minimum voltage at full load. The iW709 will turn-off the V_{BUS} switch immediately to limit the output current and reset TA to 5V. The iW709 will initiate the V_{BUS} switch soft-start and turn-off process every $T_{RECOVERY}$ if output short persists.

During normal operation when the MD is connected and the V_{BUS} switch is fully on, the voltage drop across V_{VIN} and V_{BUS} (V_{BUS} switch $R_{DS(ON)}$ IR drop) is monitored and compared with V_{OSP}. If an output short during normal operation cause V_{VIN} - V_{BUS} > V_{OSP}, iW709 will turn-off the V_{BUS} switch and CC1/CC2 current source immediately and reset TA to 5V. The iW709 will initiate the V_{BUS} switch soft-start and turn-off process every $T_{RECOVERY}$ if the output short persists.

9.10 Output Cable Soft Short Detection

The iW709 features D+/D- overvoltage protection (OVP), which addresses soft short issues in the output cables and connectors and provides protection against damages. If the voltage on the D+ or D- pin is above 4.5V, the D+/D- OVP fault is triggered. The CC1 and CC2 voltages are also monitored after IC power up. If the voltage on the CC1 or CC2 pin is above 5.6V, the CC1/CC2 OVP fault is triggered.

When the iW709 detects a D+/D-/CC1/CC2 OVP the V_{BUS} switch and the CC1/CC2 current source are disabled. Then the iW709 will reset the TA to 5V and waits for $T_{RECOVERY}$ to restart attach detection after no fault is detected.

9.11 Output Voltage/Current Regulation

The iW709 monitors the V_{BUS} voltage through reading the VIN pin voltage through a 10-bit ADC. The same ADC is also used to monitor the voltage across the output current sensing resistor. The output voltage/current information from the ADC is fed to the digital compensator for regulation control. The digital compensator compares the output voltage/current with the regulation target. The voltage regulation target at startup slowly ramps up and stays at 5V at the end of startup. The current limit at startup is set at the default current. After startup, iW709 may adjust the voltage target and current limit according to the MD's valid request.

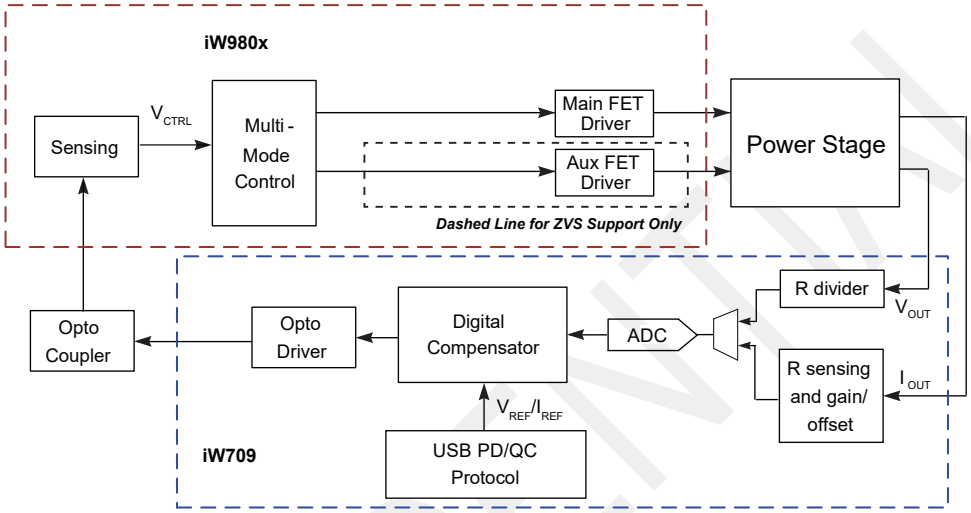


Figure 9.2 : Output Sensing and Compensator Block of iW709 in a Closed Control Loop

The iW709 decides the output regulation mode based on the voltage/current information. If the load is in normal range, the iW709 maintains a constant output voltage (CV) based on the regulation target. If the load increases beyond the acceptable range specified by the MD, the iW709 transitions to constant current (CC) mode, in which it maintains a constant output current specified by the MD and allows the output voltage to drop depending on the loading.

In either regulation mode the iW709 compares the output voltage/current to the regulation target, the difference is sent to the digital compensator to generate the proper control signal. The built-in optocoupler driver of the iW709 converts the control signal to a proper level of current going through the diode side of the optocoupler. Dialog's primary-side controller such as the iW9801/iW9809 receives this control signal through the BJT side of the optocoupler and controls the primary switch(es) accordingly to complete the closed-loop regulation.

Dialog's proprietary adaptive optocoupler driver control scheme maintains a relatively stable system gain by compensating the variation of optocoupler CTR. The built-in compensator parameter of iW709 is designed accordingly to achieve optimum regulation and dynamic performance.

9.12 Output Voltage/Current Protection

The iW709 not only uses the sampled voltage/current information for output regulation, but also for over-voltage and over-load detection. If the output voltage goes beyond the over-voltage threshold ($V_{IN(OV)}$), the iW709 enters fault state. In fault state it informs the primary controller to shut down the TA by sending the minimum optocoupler current to the primary-side. The primary-side controller will initiate the auto-restart after TA shutdown. iW709 will turn off V_{BUS} switch, reset TA to 5V and wait for $T_{RECOVERY}$ to restart the cable detection. In over-load condition, since the output current is clamped by the control loop, the output voltage drops. If the output voltage drops below a certain level, known as "CC shutdown voltage", the iW709 turns off the V_{BUS} switch and CC1/CC2 current source and resets the TA to 5V, then waits for $T_{RECOVERY}$ to restart attach detection. The CC shutdown voltage refers to the voltage at the VIN pin thus the actual shutdown voltage at MD side may vary depending on the voltage drop at the USB cable.

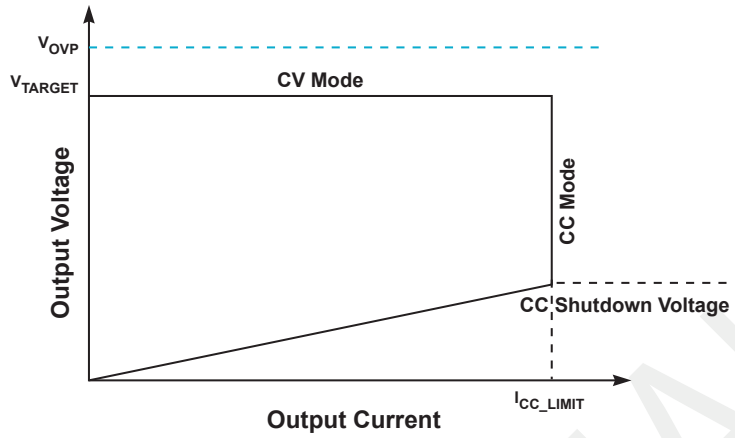


Figure 9.3 : Power Envelope

9.13 Over-Temperature Protection (OTP) and Power Derating

The iW709 has two sources for over temperature protection (OTP). One is from the IC's internal junction temperature. The other is from an external NTC resistor connected to the TS pin. The TS pin can provide an external OTP function when an NTC resistor is connected between TS and GND. An internal I_{TS} current flows though the NTC resistor and the voltage V_{TS} on the TS pin is measured by the internal ADC. The iW709 determines the NTC resistor R_{TS} value by calculating V_{TS}/I_{TS}. The NTC temperature T_{TS} is calculated by:

$$T_{TS} = \frac{1}{\left[\frac{1}{298.15} + \frac{1}{B} \times In\left(\frac{R_{SD}}{R25}\right)\right]} \quad (9.3)$$

B is material factor and R25 is the resistance of the NTC device at 25°C temperature. The iW709 monitors the NTC temperature. If the NTC temperature is higher than T_{TS_OTP}, the iW709 enters fault state and informs the primary-side to shut down the TA. The iW709 will recover to initial state if NTC temperature is below T_{TS_ST}. The B value, R25, T_{TS_ST} and T_{TS_OTP} are factory programmed. Please contact Dialog for other NTC and protection temperature configurations.

If the NTC temperature is higher than T_{TS_OTP}, iW709 will turn off V_{BUS} switch and shutdown TA by send minimum optocoupler current to the primary-side.

The iW709 also monitors the IC's junction temperature. If the IC's junction temperature is higher than T_{J_OTP}, the iW709 will turn off V_{BUS} switch and shutdown TA by send minimum optocoupler current to the primary-side.

The primary-side controller iW9801/iW9809 will initiate auto-restart after TA shutdown.

9.14 SR Powering in iW709

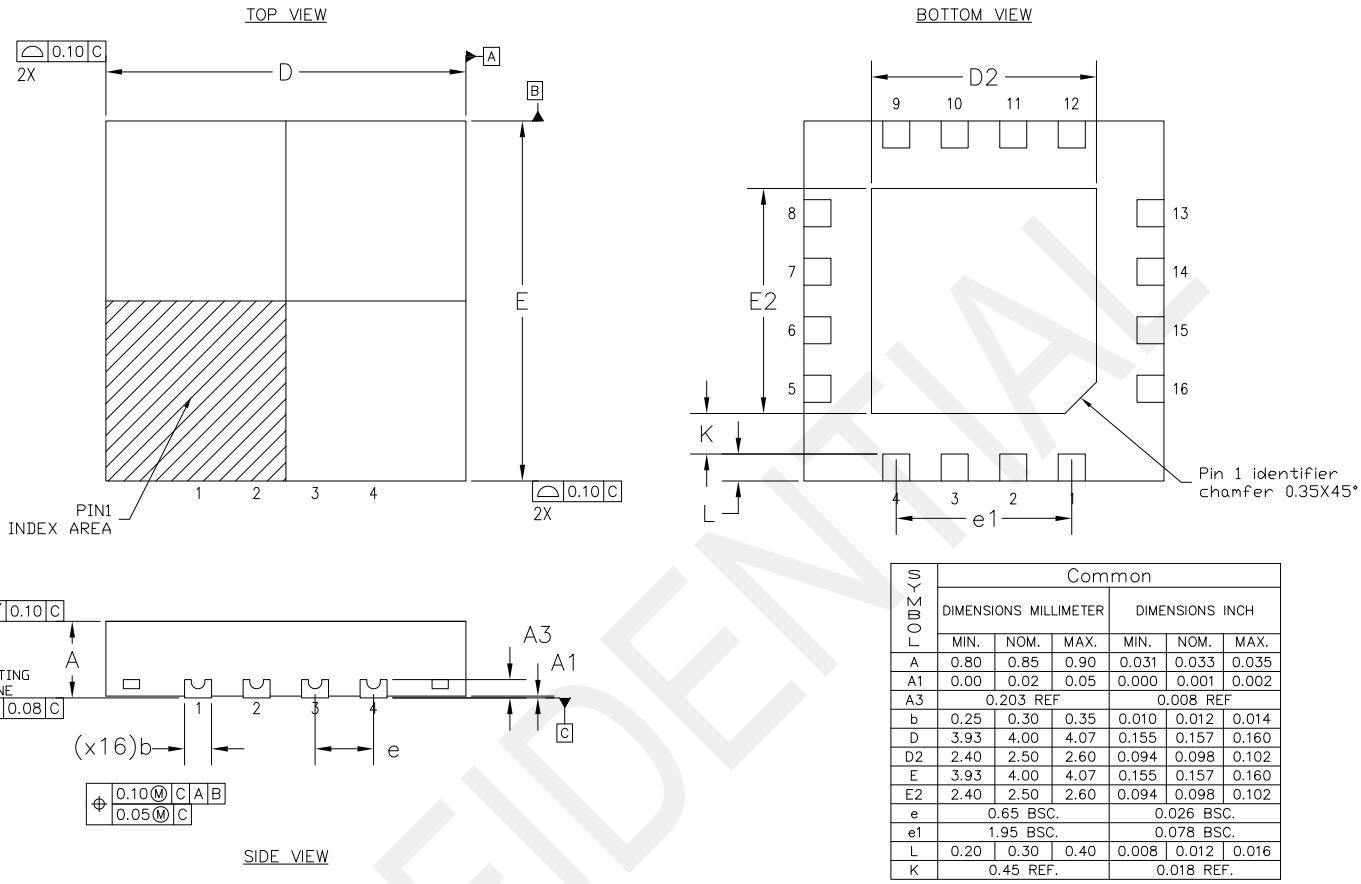
The synchronous MOSFET driver utilizes the V_{SR} voltage to pull up the MOSFET gate during SR turn-on. The V_{SR} is regulated at around 6V for optimum MOSFET driving efficiency. When TA's output voltage (V_{VIN}) is above $V_{PLR\_DISABLE}$, V_{SR} is powered by the LDO connected to the VIN pin. The LDO has a target regulation voltage at 6V. Once the TA's output voltage drops below V_{PLR_ENABLE}, the PLR regulation is enabled to maintain high level of V_{SR}. The PLR regulator mainly utilizes the high V_{DS} voltage to provide the power.

With this scheme, the iW709 always maintains sufficient V_{SR} voltage to drive the synchronous MOSFET under all output voltage and loading conditions. Thus, it is optimized for multi-level output applications from 3V to 21V.

9.15 V_{DS} Sensing and Synchronous Rectifier Driving

The synchronous rectifier (SR) control block monitors the synchronous MOSFET's drain-to-source voltage (V_{DS}) to determine the driver timing. The iW709 analyzes the V_{DS} waveform to identify the primary main switch action. It only enables SR turn-on detection when primary turn-off is confirmed. This avoids the synchronous MOSFET turn-on during transformer ringing and primary auxiliary switch on/off. When the SR turn-on is enabled, the iW709 turns on the synchronous MOSFET when the V_{DS} is below the V_{ON_TH} (-120mV), indicating that a current is going through the body diode of the synchronous MOSFET. During the SR turn on event, the control logic enables the built-in SR driver to pull up the gate voltage of the synchronous MOSFET to the V_{SR} voltage. The driver has a minimum on-time (T_{ON_MIN}) to avoid the noise from turning off the driver immediately. After the minimum on-time, the driver disables the pull-up. As the current I_{SD} decreases, V_{DS} increases and gets close to 0 mV. The SR driver is turned off when the V_{DS} reaches V_{OFF_TH}. After the SR driver turns off, the V_{DS} rises. When the V_{DS} reaches $V_{MIN\_OFF\_TH}$, the SR control block initiates a minimum off-time timer during which the SR remains off to avoid the ringing from turning on the synchronous MOSFET.

10 Physical Dimensions



SYMBOL	Common					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.203 REF			0.008 REF		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.93	4.00	4.07	0.155	0.157	0.160
D2	2.40	2.50	2.60	0.094	0.098	0.102
E	3.93	4.00	4.07	0.155	0.157	0.160
E2	2.40	2.50	2.60	0.094	0.098	0.102
e	0.65 BSC.			0.026 BSC.		
e1	1.95 BSC.			0.078 BSC.		
L	0.20	0.30	0.40	0.008	0.012	0.016
K	0.45 REF.			0.018 REF.		

11 Part Number Code Description

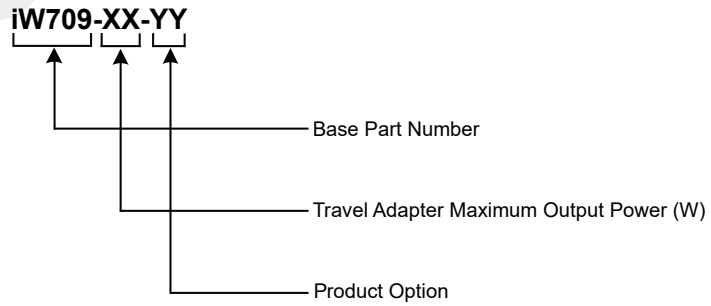


Figure 11.1 : iW709 Part Number Decoder

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Contacting Dialog Semiconductor

United Kingdom (Headquarters)
Dialog Semiconductor (UK) LTD
Phone: +44 1793 757700

Germany
Dialog Semiconductor GmbH
Phone: +49 7021 805-0

The Netherlands
Dialog Semiconductor B.V.
Phone: +31 73 640 8822

Email
info_pcbg@diasemi.com

North America
Dialog Semiconductor Inc.
Phone: +1 408 845 8500

Japan
Dialog Semiconductor K. K.
Phone: +81 3 5769 5100

Taiwan
Dialog Semiconductor Taiwan
Phone: +886 281 786 222

Web site:
www.dialog-semiconductor.com

Hong Kong
Dialog Semiconductor Hong Kong
Phone: +852 2607 4271

Korea
Dialog Semiconductor Korea
Phone: +82 2 3469 8200

China (Shenzhen)
Dialog Semiconductor China
Phone: +86 755 2981 3669

China (Shanghai)
Dialog Semiconductor China
Phone: +86 21 5424 9058