SLG74102
PCI Express Clock Generator

Features

- Two 0.7V current mode differential HCSL output pairs
- Crystal oscillator interface, 25MHz
- Output frequency: 100MHz
- Period jitter: TBD
- Output skew: 150ps (maximum)
- Cycle-to-cycle jitter: 50ps (maximum)
- I^2C support with readback capabilities up to 400kHz
- Spread Spectrum for electromagnetic interference (EMI)
- reduction
- 3.3V operating supply mode
- -40×C to 85×C ambient operating temperature
- Available in both standard and lead-free RoHS compliant
- packages

General Description

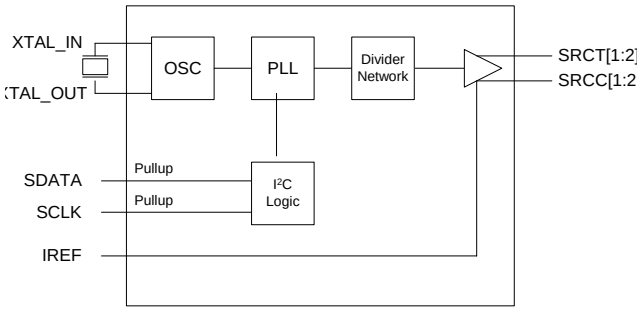
The SLG74102 is a member of Silego's PCI Express Gen 2 family. Consult Silego Marketing for details.

The SLG74102 is a PLL-based clock generator specifically designed for PCI_Express™Clock Generation applications. This device generates a 100MHz HCSL clock. The device offers a HCSL (Host Clock Signal Level) clock output from a clock input reference of 25MHz. The input reference may be derived from an external source or by the addition of a 25MHz crystal to the on-chip crystal oscillator. An external reference may be applied to the XTAL_IN pin with the XTAL_OUT pin left floating.

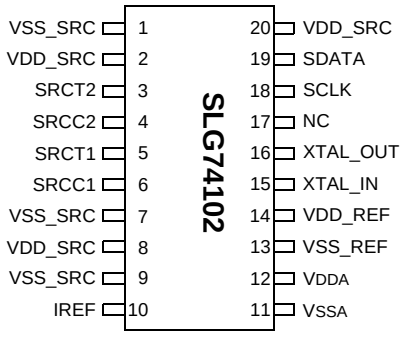
The device offers spread spectrum clock output for reduced EMI applications. An I2C bus interface is used to enable or disable spread spectrum operation as well as select either a down spread value of -0.35% or -.5%.

The SLG74102 is available in both standard and lead-free 20-Lead TSSOP packages.

Block Diagram



Pin Assignment



20-pin TSSOP

6.5mm x 4.4mm x 0.92mm
package body
G Package
Top View

Table 1. Pin Descriptions

Pin #	Name	Type	Description
1,7,9	V_{SS_SRC}	Power	Ground for SRC outputs
2,8,20	V_{DD_SRC}	Power	Power supply for SRC outputs
3	SRCT2	Output	Differential output pair. HCSL interface levels
4	SRCC2	Output	Differential output pair. HCSL interface levels
5	SRCT1	Output	Differential output pair. HCSL interface levels
6	SRCC1	Output	Differential output pair. HCSL interface levels
10	IREF	Input	A fixed precision resistor (475 Ω) from this pin to ground provides a reference current used for differential current-mode SRCCx, SRCTx clock ouputs.
11	V_{SSA}	Power	Analog ground pin.
12	V_{DDA}	Power	Power supply for PLL
13	V_{SS_REF}	Power	Ground for crystal interface
14	V_{DD_REF}	Power	Power supply for crystal interface
15,16	XTAL_IN, XTAL_OUT	Input	Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output
17	NC	Unused	No connect
18	SCLK	Input, Pul-lup	SMBus compatible SCLK. This pin has an internal pullup resistor. LVCMOS/LVTTL interface levels.
19	SDATA	I/O Pullup	SMBus compatible SDATA. This pin has an internal pullup resistor. LVCMOS/LVTTL interface levels.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
C_{OUT}	Output Pin Capacitance		3		5	pF
L_{IN}	Pin Inductance				7	nH

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore, use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in Table 3A. The block write and block read protocol is outlined in Table 3B, while Table 3C outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 3A. Command Code Definition

BIT	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation.
6:5	Chip select address, set to “00” to access device.
4:0	Byte offset for byte read or byte write operation. For block read and block write operations, these bits must be “00000”.

Table 3B. Block Read and Block Write Protocol

BIT	Description = Block Write	BIT	Description = Block Read
1	Start	1	Start
2:8	Slave address - 7 bit	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits	11:18	Command Code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 0-8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1-8 bits	30:37	Byte Count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
	Data Btye/ Slave Acknowledges	39:46	Data Byte 1 from slave - 8 bits
	Data Byte N - 8 bits	47	Acknowledge
	Acknowledge from slave	48:55	Data Byte 2 from slave - 8 bits
	Stop	56	Acknowledge
			Data Bytes from Slave / Acknowledges
			Data Byte from slave - 8 bits
			Not Acknowledge

Table 3C. Byte Read and Byte Write Protocol

BIT	Description = Block Write	BIT	Description = Block Read
1	Start	1	Start
2:8	Slave address - 7 bit	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits	11:18	Command Code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Byte Count from slave - 8 bits
		38	Acknowledge
		39	Stop

Control Registers

Byte 0: Control Register 0

BIT	@Pup	Name	Description
7	0	Reserved	Reserved
6	1	Reserved	Reserved
5	1	Reserved	Reserved
4	1	SRC[T/C]2	SRC[T/C]2 Output Enable 0 = Disalbe (Hi-Z) 1 = Enable
3	1	SRC[T/C]1	SRC[T/C]1 Output Enable 0 = Disable (Hi-Z) 1 = Enable
2	1	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Table 4B. Byte 1: Control Register 1

BIT	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Table 4C. Byte 2: Control Register 2

BIT	@Pup	Name	Description
7	1	SRCT/C	Spread Spectrum Selection 0 = -.35%, 1 = -0.50%
6	1	Reserved	Reserved
5	1	Reserved	Reserved
4	0	Reserved	Reserved
3	1	Reserved	Reserved
2	0	SRC	SRC Spread Spectrum Enable 0 = Spread Off, 1 = Spread On
1	1	Reserved	Reserved
0	1	Reserved	Reserved

Table 4D. Byte 3: Control Register 3

BIT	@Pup	Name	Description
7	1	Reserved	Reserved
6	0	Reserved	Reserved
5	1	Reserved	Reserved
4	0	Reserved	Reserved
3	1	Reserved	Reserved
2	1	Reserved	Reserved
1	1	Reserved	Reserved
0	1	Reserved	Reserved

Table 4E. Byte 4: Control Register 4

BIT	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	1	Reserved	Reserved

Table 4F. Byte 5: Control Register 5

BIT	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Table 4G. Byte 6: Control Register 6

BIT	@Pup	Name	Description
7	0	TEST_SEL	REF or Tri-state Select 0 = Hi-Z, 1 = REF
6	0	TEST_MODE	TEST Clock Mode Entry Control 0 = Normal Operation, 1 = REF or Hi-Z Mode
5	0	Reserved	Reserved
4	1	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	1	Reserved	Reserved
0	1	Reserved	Reserved

Table 4H. Byte 7: Control Register 7

BIT	@Pup	Name	Description
7	0		Revision Code Bit 3
6	0		Revision Code Bit 2
5	0		Revision Code Bit 1
4	0		Revision Code Bit 0
3	0		Vendor ID Bit 3
2	1		Vendor ID Bit 2
1	1		Vendor ID Bit 1
0	0		Vendor ID Bit 0

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Output Driver Current

The SLG74102 outputs are HCSL current drive with the current being set with a resistor from IREF to ground. For a 50Ω pc board trace, the drive current would typically be set with a RREF of 475Ω which products an IREF of 2.32mA. The IREF is multiplied by a current mirror to an output drive of 6*2.32mA or 13.92mA. See *Figure 1* for current mirror and output drive details

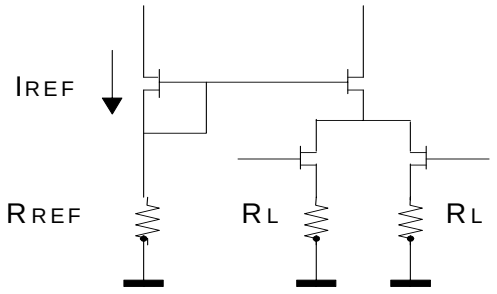


Figure 1. HSCL Current Mirror and Output Driver

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performace, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL)

Figure 2 shows how typical crystal configuration using the two trim capacitors. An important clairification for the following discussing is that the trim capacitors are in series with the crystal not parallel. It is a common misconception that load capacitors in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is not true.

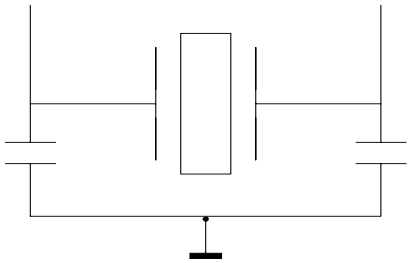


Figure 2. Crystal Capacitive Clarification

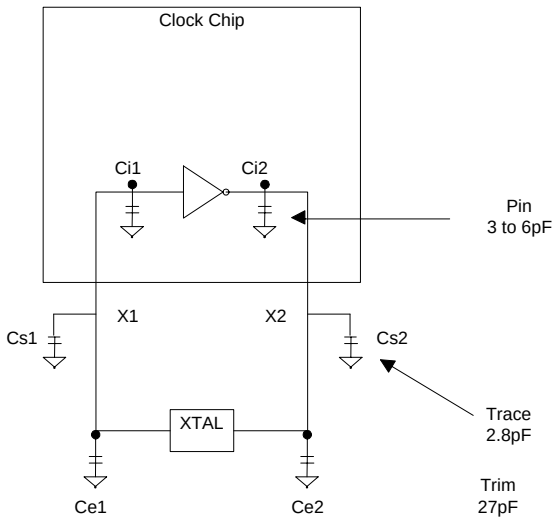


Figure 3. Crystal Loading Example

Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Load Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce + Cs + Ci} + \frac{1}{2Ce + 2Cs + 2Ci}\right)}$$

CL.....Crystal load capacitance

CLe.....Actual loading seen by crystal using standard value trim capacitors

Ce.....External trim capacitors

Cs.....Stray capacitance (terraced)

Ci.....Internal capacitance (lead frame, bond wires, etc.)

Calculating Load Capacitors

In addition to the standard trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the

crystal must be twice the specificed crystal load capacitance (CL). While the capacitance on each side of the crystal is a series with the crystal, trim capacitors (Ce1, Ce2) should be calculated to provide equal loading on both sides.

Crystal Recommendations

The SLG74102 requires a parallel resonance crystal. Substituting a series resonance crystal will cause the SLG74102 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300ppm frequency shift between series and parallel crystals due to incorrect loading.

Table 5. Crystal Recommendation Table

Frequency (Fund)	Cut	Loading	Load Cap	Drive (Max.)	Shunt Cap (Max.)	ESR (Max.)	Rise/Fall Time	Tolerance (Max.)	Stability (Max.)	Aging (Max.)
25 MHz	At	Parallel	12pF - 16pF	1mW	7pF	50Ω	10ns	±50ppm	±50ppm	5ppm

Absolute Maximum Ratings

Supply Voltage, V_{DD} 4.6V

Inputs, V_I -0.5V to V_{DD_REF} + 0.5 V

Outputs, V_O -0.5V to V_{DD_SRC} + 0.5V

Package Thermal Impedance, θ_{JA} 73.2°C/W (0 lfpm)

Storage Temperature, T_{STG} -65°C to 150°C

NOTE:

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 6A. Power Supply DC Characteristics, VDD_REF = VDDA = VDD_SRC = 3.3V ±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDD_REF	Power Supply Voltage		3.135	3.3	3.465	V
VDDA	Analog Supply Voltage		3.135	3.3	3.465	V
VDD_SRC	Output Supply Voltage		3.135	3.3	3.465	V
IDD	Dynamic Supply Current	At Max. Load and Frequency			400	mA
IDDA	Analog Supply Current			TBD		mA

Table 6B. DC Characteristics, VDD_REF = VDDA =VDD_SRC = 3.3V ±5%, TA = -40°C to 85°C

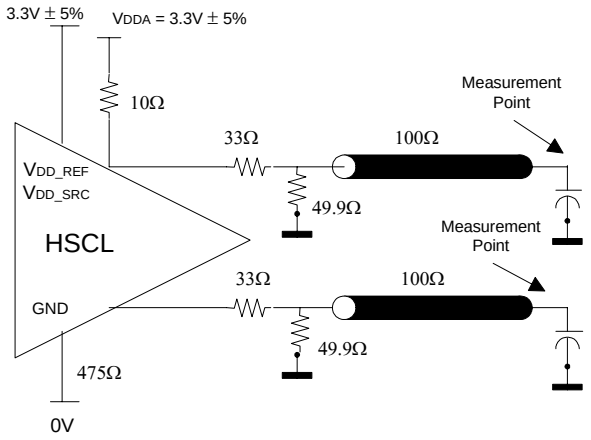
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIHSMBUS	Input High Voltage	SDATA, SCLK		2.2			V
VILSMBUS	Input Low Voltage	SDATA, SCLK				1.0	V
IIH	Input High Current	SDATA, SCLK	VDD = VIN = 3.465V			5	µA
IIL	Input Low Current	SDATA, SCLK	VDD = 3.465V,VIN = 0V	-150			µA
IOH	Output Current				14		mA
IOZ	High Impedance Leakage Current			-10		10	µA

Table 7. AC Characteristics, VDD_REF = VDDA = VDD_SRC = 3.3V ±5%, TA = -40°C to 85°C

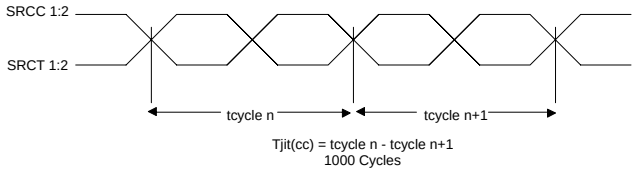
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
fref	Frequency				25		MHz
sclk	SCLK Frequency					400	kHz
	Frequency Tolerance NOTE1;	XTAL				50	ppm
		External Reference				0	ppm
odc	SRCT/SRCC Duty Cycle; NOTE 2			45		55	%
tsk(o)	SRCT/C to SRCT/C Clock Skew; NOTE 2					150	ps
tPERIOD	Average Period; NOTE 3			9.9970		10.0533	ns
tjit(cc)	SRCT/C Cycle-to-Cycle Jitter; NOTE 2					50	ps
tR / tF	SRCT/SRCC Rise/Fall Time; NOTE 4			175		700	ps
tRFM	Rise/Fall Time Matching; NOTE 5					20	%
tDC	XTAL_IN Duty Cycle; NOTE 6			47.5		52.5	%
∆tR/tF	Rise/Fall Time Variation					125	ps
VHIGH	Voltage High			660		850	mV
VLOW	Voltage Low			-150			mV
VOX	Output Crossover Voltage		@ 0.7V Swing	250		550	mV
VOVS	Maximum Overshoot Voltage					VHIGH + 0.3	V
VUDS	Minimum Undershoot Voltage			-0.3			V
VRB	Ring Back Voltage					0.2	V

NOTE 1: With recommended crystal.
NOTE 2: Measure at crossing point VOX.
NOTE 3: Measure at crossing point VOX at 100MHz.
NOTE 4: Measured from VOL = 0.175V to VOH = 0.525V.
NOTE 5: Determined as a fraction of 2*(tR - tF) / (tR + tF).
NOTE 6: the device will operate reliably with input duty cycles up to 30/70% but the REF clock duty cycle will not be within specification.

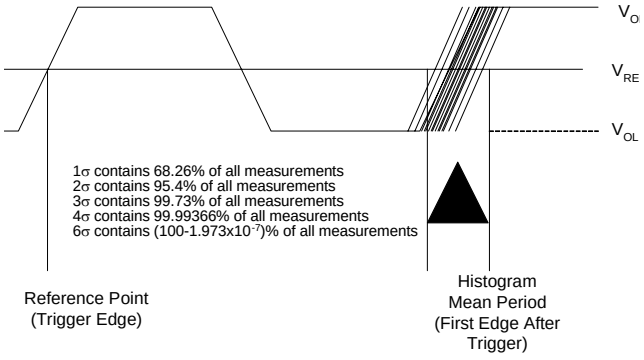
Parameter Measurement Information



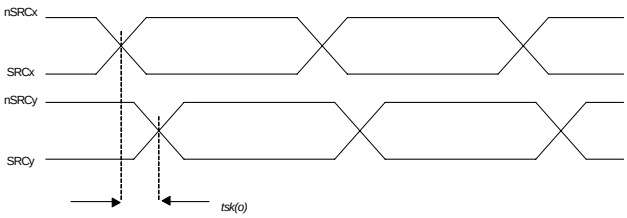
3.3V HCSL Output Load AC Test Circuit



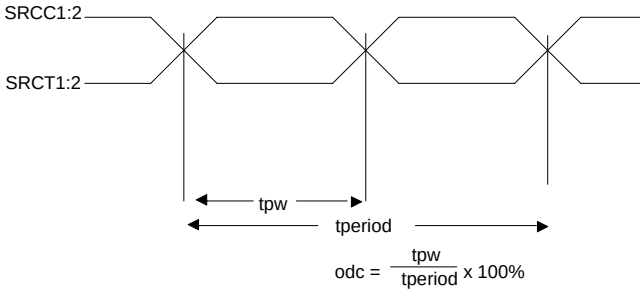
Cycle-to-Cycle Jitter



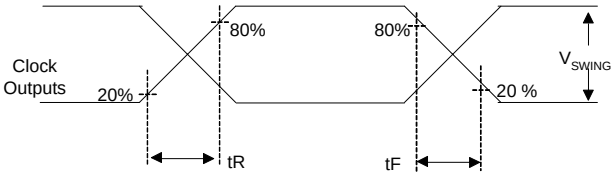
Period Jitter



Output Skew



Output Duty Cycle/Pulse Width/Period



HCSL Output Rise/Fall Time

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The SLG74102 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. VDD_REF, VDDA, and VDD_SRC should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 4* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each VDDA. The 10Ω resistor can also be replaced by a ferrite bead.

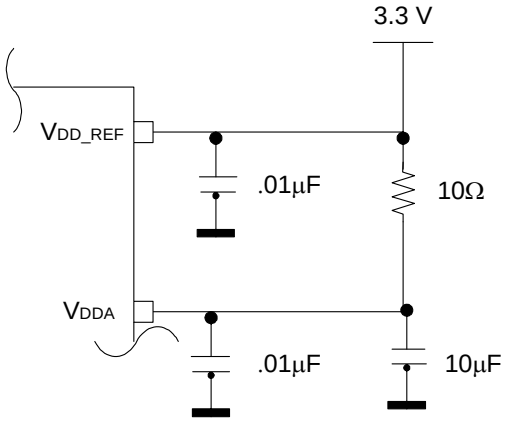


Figure 4. Power Supply Filtering

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

HCSL Output
All unused HCSL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 20 Lead TSSOP

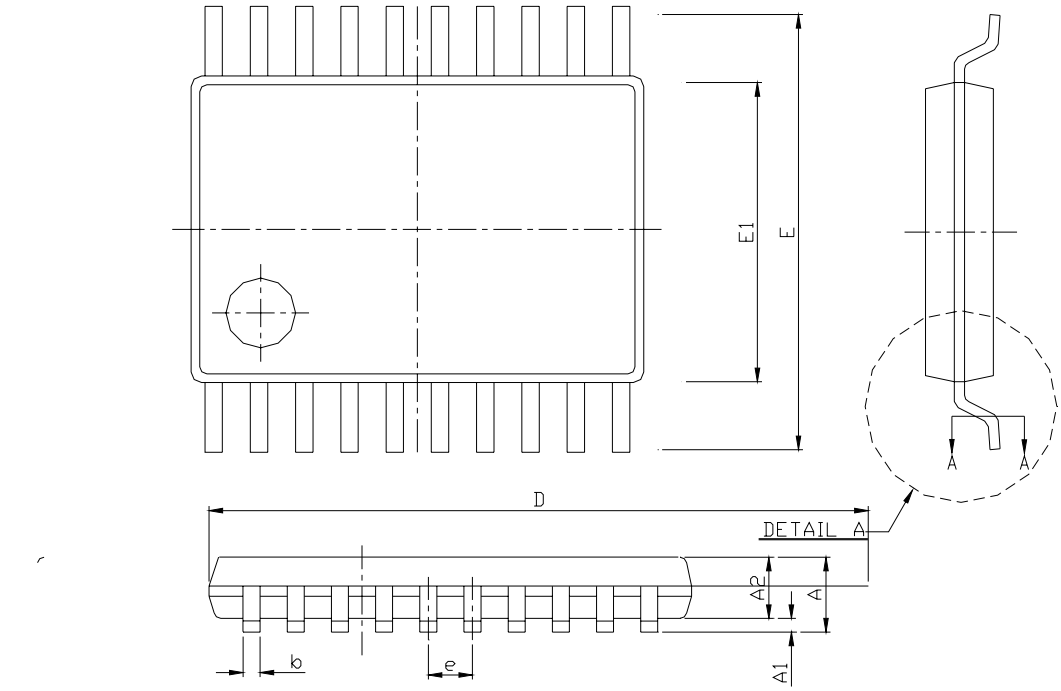
	θ_{JA} by Velocity (Linear Feet per Minute)		
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

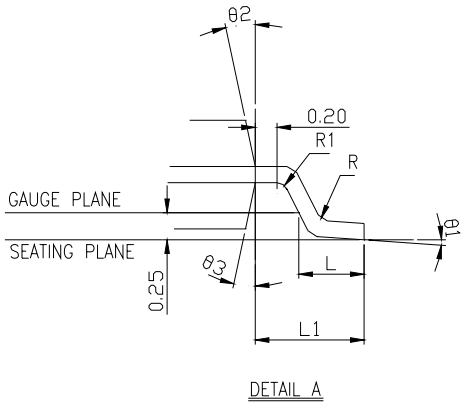
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

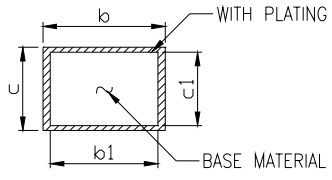
The transistor count for SLG74102 is: TBD

Package Outline - G Suffix for 20 Lead TSSOP





DETAIL A



SECTION A–A

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.20			0.043
A1	0.05		0.15	0.002		0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
L	0.50	0.60	0.75	0.020	0.024	0.030
E	6.40 BSC.			0.252 BSC.		
E1	4.30	4.40	4.50	0.169	0.173	0.177
R	0.09			0.004		
R1	0.09			0.004		
b	0.19		0.30	0.007		0.012
b1	0.19	0.22	0.25	0.007	0.009	0.010
c	0.09		0.20	0.004		0.008
c1	0.09		0.16	0.004		0.006
L1	1.0 REF.			0.039 REF.		
e	0.65 BSC.			0.026 BSC.		
θ1	0		8	0		8
θ2	12 REF.			12 REF.		
θ3	12 REF.			12 REF.		

	D (MM)			JEDEC
N	MIN.	NOM	MAX.	
20	6.40	6.50	6.60	MO-153 (AC)