# SLG5NT1734V

## Ultra-small 28.5 mΩ, 1.0 A Integrated Power Switch with Discharge

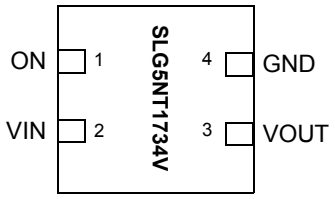
### General Description

The SLG5NT1734V is designed for load switching applications with ultra low quiescent current. The part comes with one 28.5 mΩ 1.0 A rated P-channel MOSFET controlled by a single ON control pin. The product is packaged in an ultra-small 1.0 x 1.0 mm package.

### Features

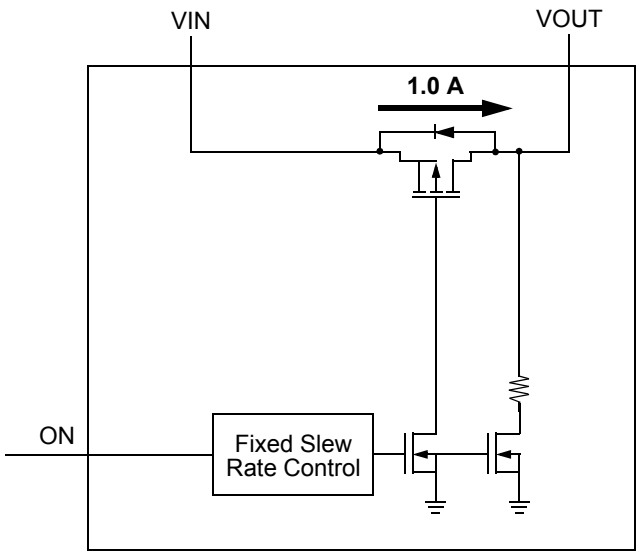
- One 1.0 A MOSFET
- Ultra Low Quiescent Current
- Low $RDS_{ON}$
  - 28.5 mΩ @ 5.0 V
  - 36.4 mΩ @ 3.3 V
  - 44.3 mΩ @ 2.5 V
  - 60.8 mΩ @ 1.8 V
  - 77.6 mΩ @ 1.5 V
- $V_{IN}$ = 1.5 V to 5.0 V
- Integrated Discharge Resistor
- Pb-Free / Halogen-Free / RoHS compliant
- STDFN 4L, 1.0 x 1.0 x 0.55 mm

### Pin Configuration




**4-pin STDFN**
(Top View)

### Block Diagram



## Pin Description

| Pin # | Pin Name | Type | Pin Description |
|---|---|---|---|
| 1 | ON | Input | Turns on MOSFET, active high |
| 2 | VIN | MOSFET | Power MOSFET input |
| 3 | VOUT | MOSFET | Power MOSFET output |
| 4 | GND | GND | Ground |

## Ordering Information

| Part Number | Type | Production Flow |
|---|---|---|
| SLG5NT1734V | STDFN 4L | Industrial, -40 °C to 85 °C |
| SLG5NT1734VTR | STDFN 4L (Tape and Reel) | Industrial, -40 °C to 85 °C |

## Absolute Maximum Ratings

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Power Switch Input Voltage | | -- | -- | 6 | V |
| $T_S$ | Storage Temperature | | -65 | -- | 140 | °C |
| $ESD_{HBM}$ | ESD Protection | Human Body Model | 2000 | -- | -- | V |
| $ESD_{CDM}$ | ESD Protection | Charged Device Model | 1000 | -- | -- | V |
| MSL | Moisture Sensitivity Level | | 1 | | | |
| $\theta_{JA}$ | Package Thermal Resistance, Junction-to-Ambient | 1 mm x 1 mm STDFN; Determined using 1 $in^2$, 1.2 oz. copper pads under VIN and VOUT on FR4 pcb material | -- | 122 | -- | °C/W |
| $W_{DIS}$ | Package Power Dissipation | | -- | -- | 0.5 | W |
| MOSFET $IDS_{PK}$ | Peak Current from Drain to Source | For no more than 1 ms with 1% duty cycle | -- | -- | 1.5 | A |

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Electrical Characteristics

$T_A$ = -40 °C to 85 °C (unless otherwise stated)

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Power Switch Input Voltage | -40 °C to 85 °C | 1.5 | -- | 5.0 | V |
| $I_{IN}$ | Power Switch Current (PIN 2) | when OFF, $V_{IN}$ = 5.0 V | -- | 0.03 | 1 | µA |
| | | when ON = $V_{IN}$, No load | -- | 0.05 | 0.5 | µA |
| $I_{ON\_LKG}$ | ON Pin Input Leakage | | -- | -- | 0.1 | µA |
| $RDS_{ON}$ | ON Resistance @ $T_A$ 25°C | @ 5.0 V, 100 mA | -- | 28.5 | 37 | mΩ |
| | | @ 3.3 V, 100 mA | -- | 36.4 | 45 | mΩ |
| | | @ 2.5 V, 100 mA | -- | 44.3 | 54 | mΩ |
| | | @ 1.8 V, 100 mA | -- | 60.8 | 73.5 | mΩ |
| | | @ 1.5 V, 100 mA | -- | 77.6 | 93.2 | mΩ |
| $RDS_{ON}$ | ON Resistance @ $T_A$ 85°C | @ 5.0 V, 100 mA | -- | 34 | 43.6 | mΩ |
| | | @ 3.3 V, 100 mA | -- | 43.8 | 53.6 | mΩ |
| | | @ 2.5 V, 100 mA | -- | 53.3 | 64.3 | mΩ |
| | | @ 1.8 V, 100 mA | -- | 72.2 | 86 | mΩ |
| | | @ 1.5 V, 100 mA | -- | 90.7 | 107.2 | mΩ |
| MOSFET IDS | Current from VIN to VOUT | Continuous | -- | -- | 1.0 | A |
| $T_{ON\_Delay}$ | ON pin Delay Time | 50% ON to Ramp Begin $V_{IN}$ = 5.0 V, $C_{LOAD}$ = 0.1 µF, $R_{LOAD}$ = 10 Ω | 0.4 | 1.1 | 2.2 | ms |
| | | 50% ON to Ramp Begin $V_{IN}$ = 3.3 V, $C_{LOAD}$ = 0.1 µF, $R_{LOAD}$ = 10 Ω | 0.56 | 1.3 | 2.6 | ms |
| | | 50% ON to Ramp Begin $V_{IN}$ = 1.5 V, $C_{LOAD}$ = 0.1 µF, $R_{LOAD}$ = 10 Ω | 0.73 | 1.8 | 3.35 | ms |

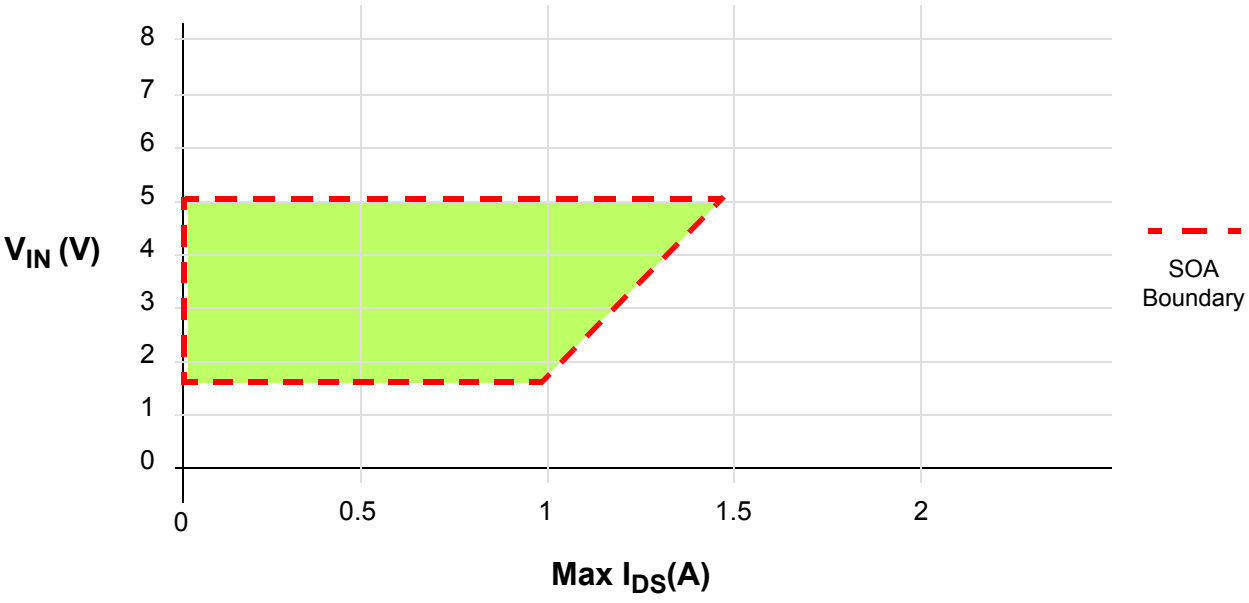
## Electrical Characteristics (continued)

$T_A$ = -40 °C to 85 °C (unless otherwise stated)

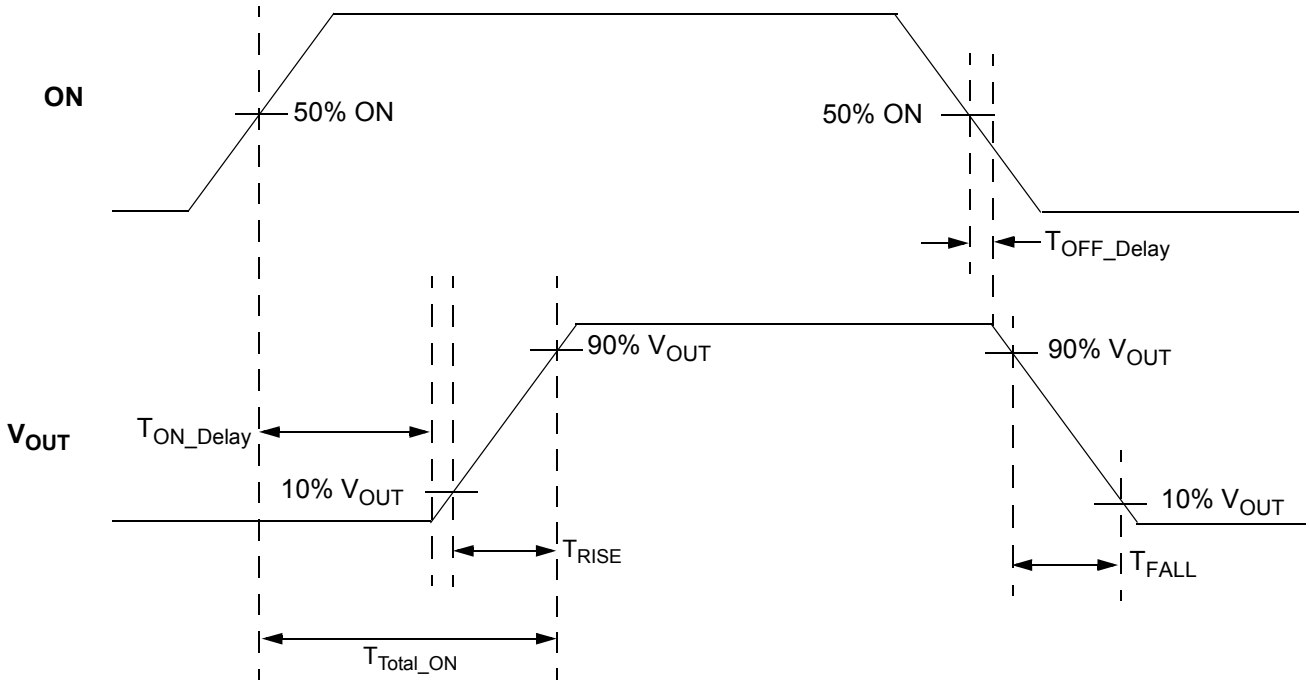
| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{Total\_ON}$ | Total Turn On Time | 50% ON to 90% $V_{OUT}$<br>$V_{IN}$ = 5.0 V, $C_{LOAD}$ = 0.1 µF,<br>$R_{LOAD}$ = 10 Ω | 2.12 | 3.7 | 6.18 | ms |
| | | 50% ON to 90% $V_{OUT}$<br>$V_{IN}$ = 3.3 V, $C_{LOAD}$ = 0.1 µF,<br>$R_{LOAD}$ = 10 Ω | 2.04 | 3.6 | 6.18 | ms |
| | | 50% ON to 90% $V_{OUT}$<br>$V_{IN}$ = 1.5 V, $C_{LOAD}$ = 0.1 µF,<br>$R_{LOAD}$ = 10 Ω | 1.97 | 3.2 | 5.61 | ms |
| $T_{RISE}$ | Rise Time | 10% $V_{OUT}$ to 90% $V_{OUT}$<br>$V_{IN}$ = 5.0 V, $C_{LOAD}$ = 0.1 µF,<br>$R_{LOAD}$ = 10 Ω | 1.40 | 2.30 | 3.63 | ms |
| | | 10% $V_{OUT}$ to 90% $V_{OUT}$<br>$V_{IN}$ = 3.3 V, $C_{LOAD}$ = 0.1 µF,<br>$R_{LOAD}$= 10 Ω | 1.1 | 1.91 | 3.1 | ms |
| | | 10% $V_{OUT}$ to 90% $V_{OUT}$<br>$V_{IN}$ = 1.5 V, $C_{LOAD}$ = 0.1 µF,<br>$R_{LOAD}$ = 10 Ω | 0.79 | 1.30 | 2.2 | ms |
| $R_{DIS}$ | Discharge Resistance | $V_{IN}$ = 1.5 V to 5.0 V, $V_{OUT}$ = 0.4 V<br>Input Bias | 46 | 96 | 250 | Ω |
| ON_$V_{IH}$ | Initial Turn On Voltage | | 0.85 | -- | $V_{IN}$ | V |
| ON_$V_{IL}$ | Low Input Voltage on ON pin | | -0.3 | 0 | 0.3 | V |
| $T_{OFF\_Delay}$ | OFF Delay Time | 50% ON to $V_{OUT}$ Fall Start,<br>$V_{IN}$ = 5.0 V, $R_{LOAD}$ =10 Ω, no $C_{LOAD}$ | 4.56 | 5.9 | 7.44 | µs |

Notes:
1. $V_{IN}$ ≥ 2 V, linear and monotonic power on ramp.(*Figure 11*)
2. $V_{IN}$ < 2 V with 2 Ω load, non-linear and monotonic power on ramp. (*Figure 10*, $V_{IN}$ = 1.5 V, $C_{LOAD}$ = 0.1 µF, $R_{LOAD}$ = 1.5 Ω)

### $V_{IN}$ vs. Max $I_{DS}$, Safe Operation Area



### $T_{Total\_ON}$, $T_{ON\_Delay}$ and Slew Rate Measurement




Note: Rise and Fall times of the ON signal are 100 ns

## Typical Turn-on Waveforms

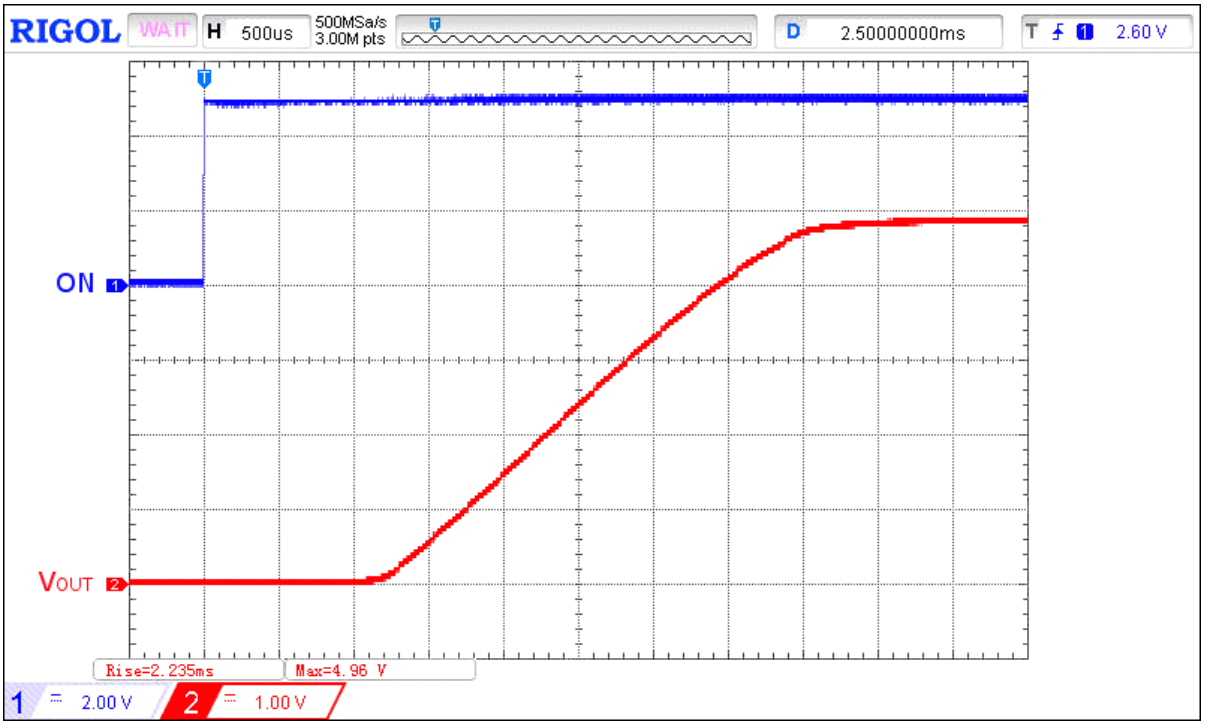



**Figure 1. Typical Turn ON operation waveform for $V_{IN}$ = 5 V, $C_{LOAD}$ = 0.1 µF, $R_{LOAD}$ = 10 Ω**

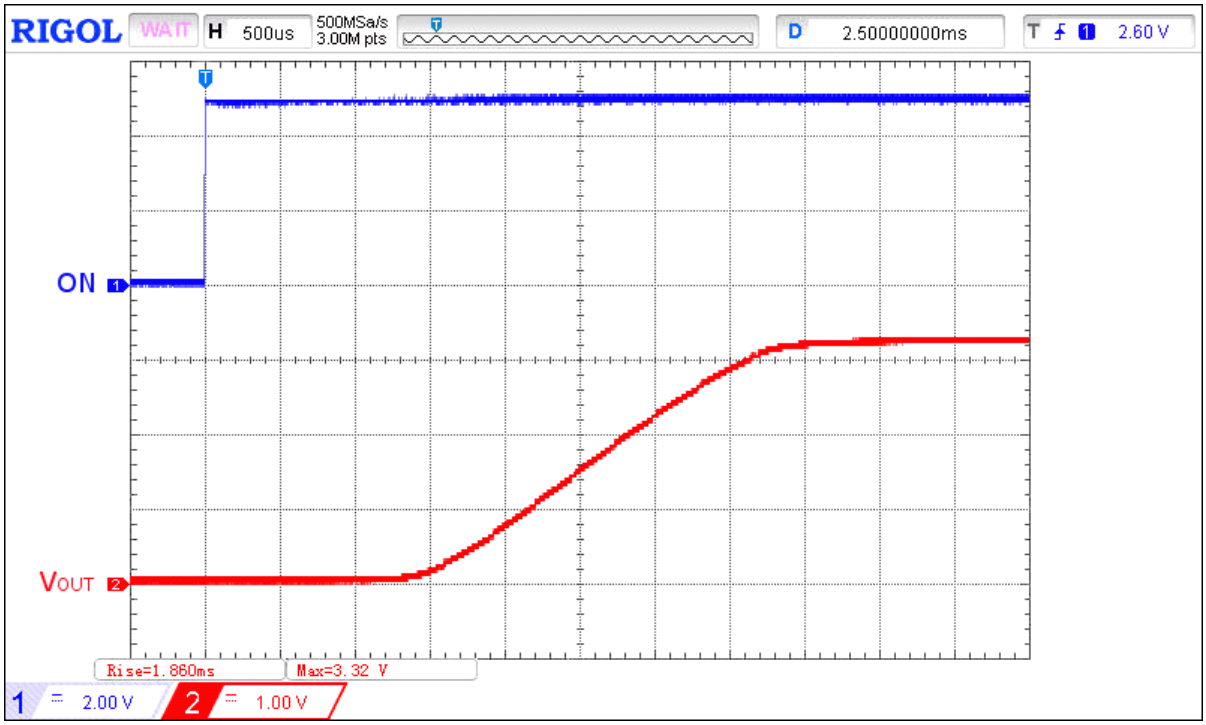



**Figure 2. Typical Turn ON operation waveform for $V_{IN}$ = 3.3 V, $C_{LOAD}$ = 0.1 µF, $R_{LOAD}$ = 10 Ω**

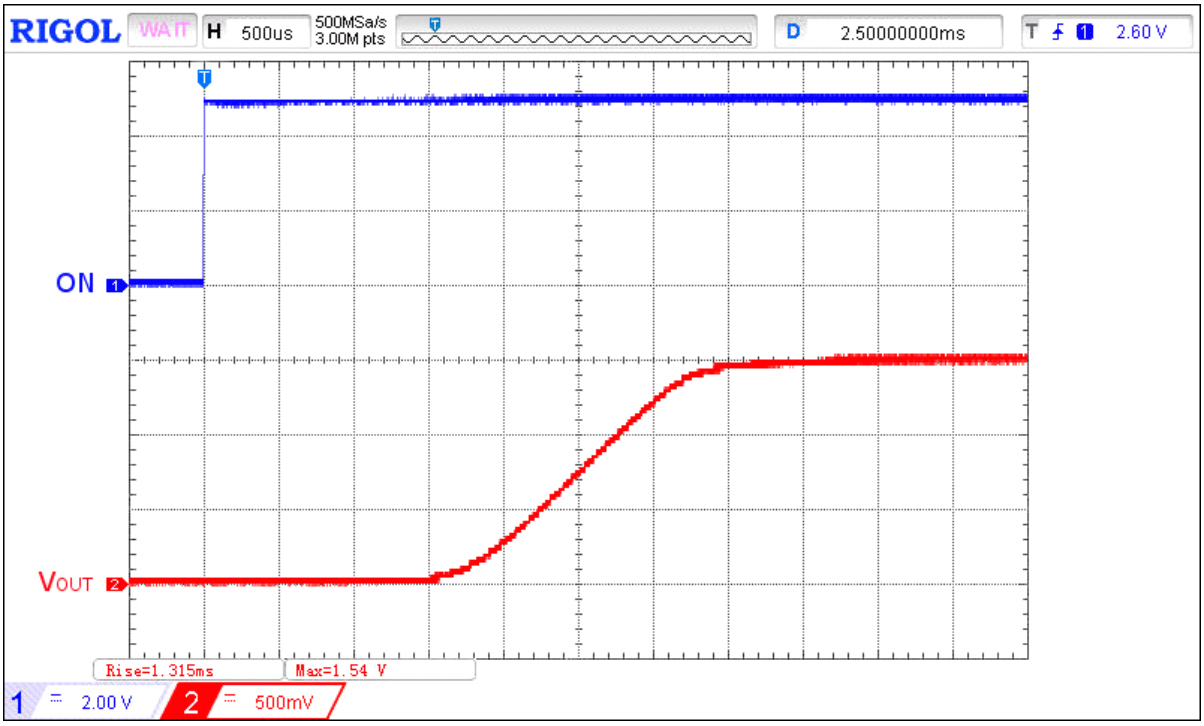



**Figure 3. Typical Turn ON operation waveform for $V_{IN}$ = 1.5 V, $C_{LOAD}$ = 0.1 µF, $R_{LOAD}$ = 10 Ω**

## Typical Turn-off Waveforms

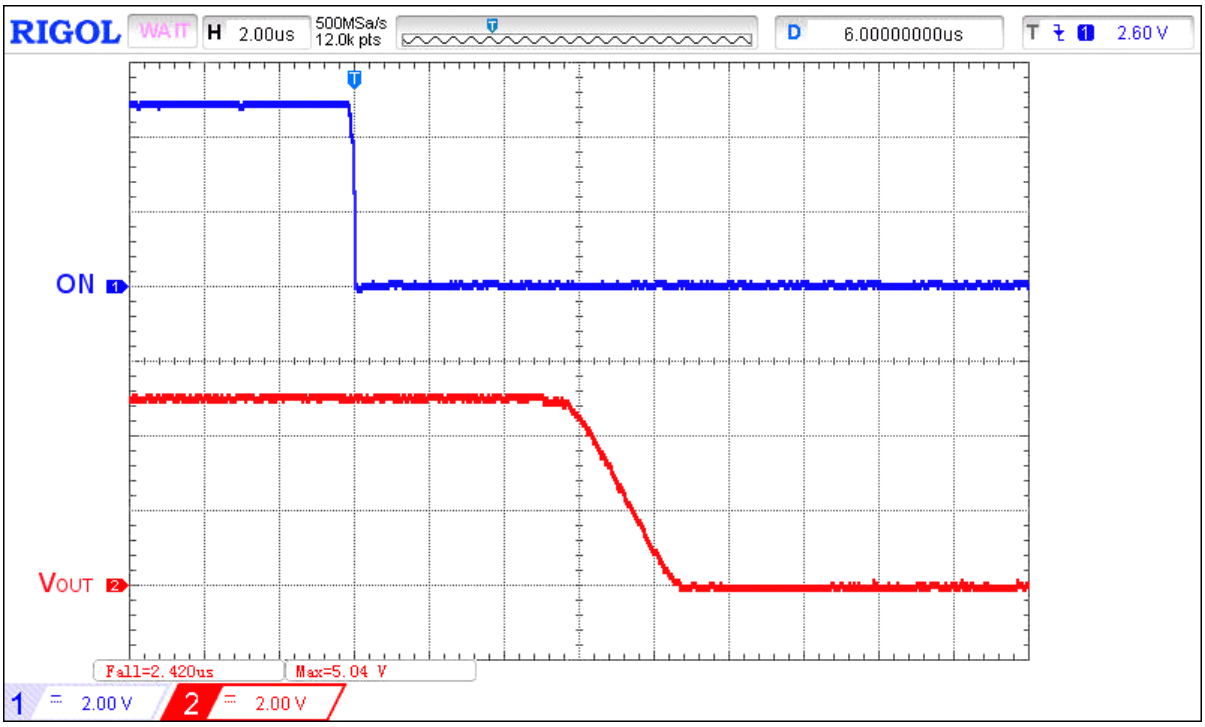



**Figure 4. Typical Turn OFF operation waveform for $V_{IN}$ = 5 V, no $C_{LOAD}$ , $R_{LOAD}$ = 10 Ω**

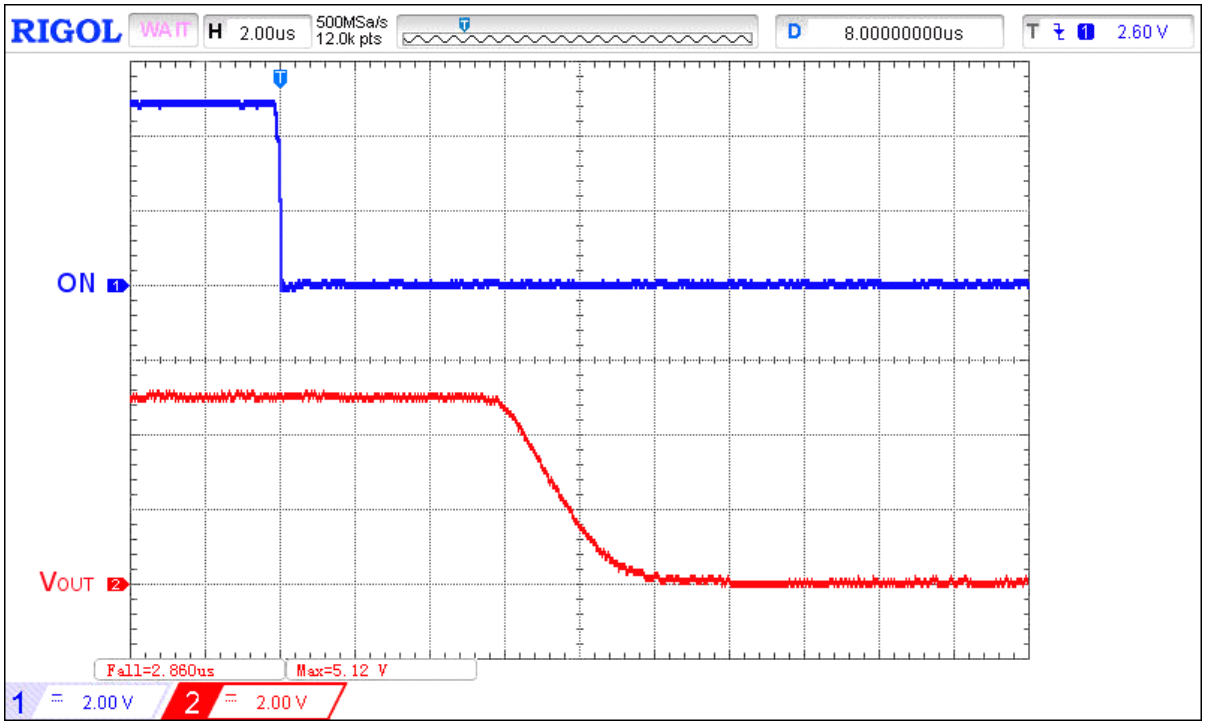



**Figure 5. Typical Turn OFF operation waveform for $V_{IN}$ = 5 V, $C_{LOAD}$ = 0.1 µF, $R_{LOAD}$ = 10 Ω**

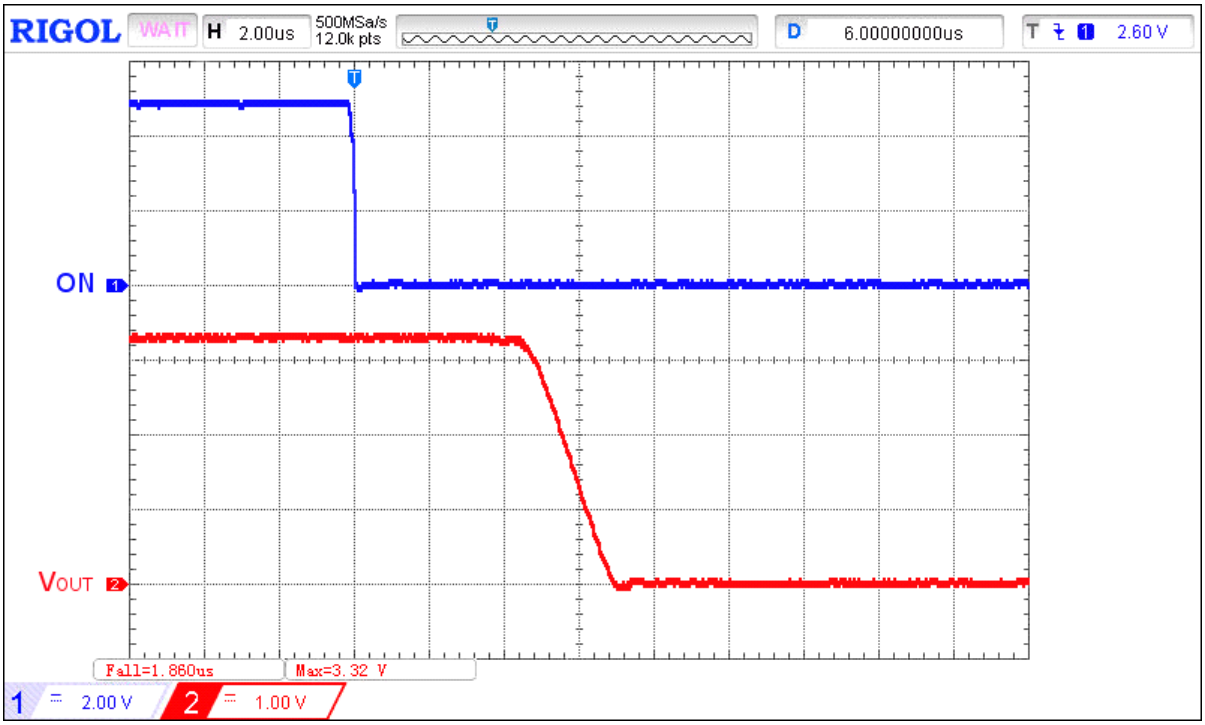



**Figure 6. Typical Turn OFF operation waveform for $V_{IN}$ = 3.3 V, no $C_{LOAD}$ , $R_{LOAD}$ = 10 Ω**

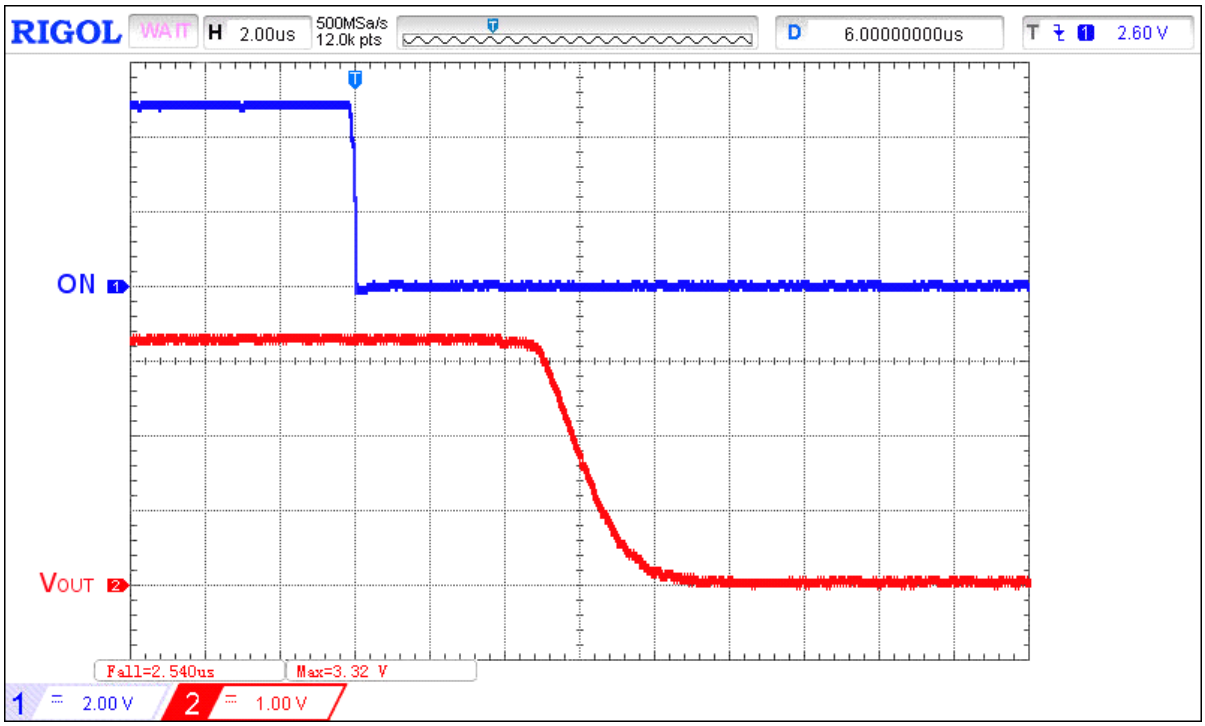



**Figure 7. Typical Turn OFF operation waveform for $V_{IN}$ = 3.3 V, $C_{LOAD}$ = 0.1 µF, $R_{LOAD}$ = 10 Ω**

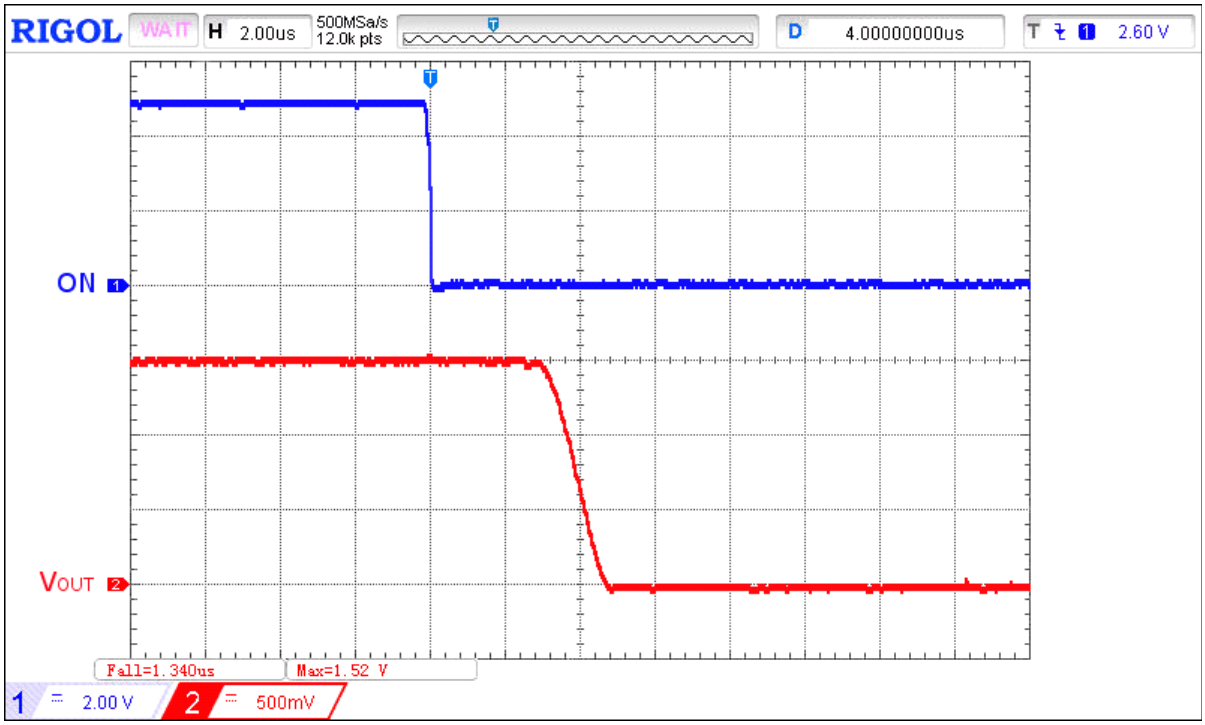



**Figure 8. Typical Turn OFF operation waveform for $V_{IN}$ = 1.5 V, no $C_{LOAD}$ , $R_{LOAD}$ = 10 Ω**

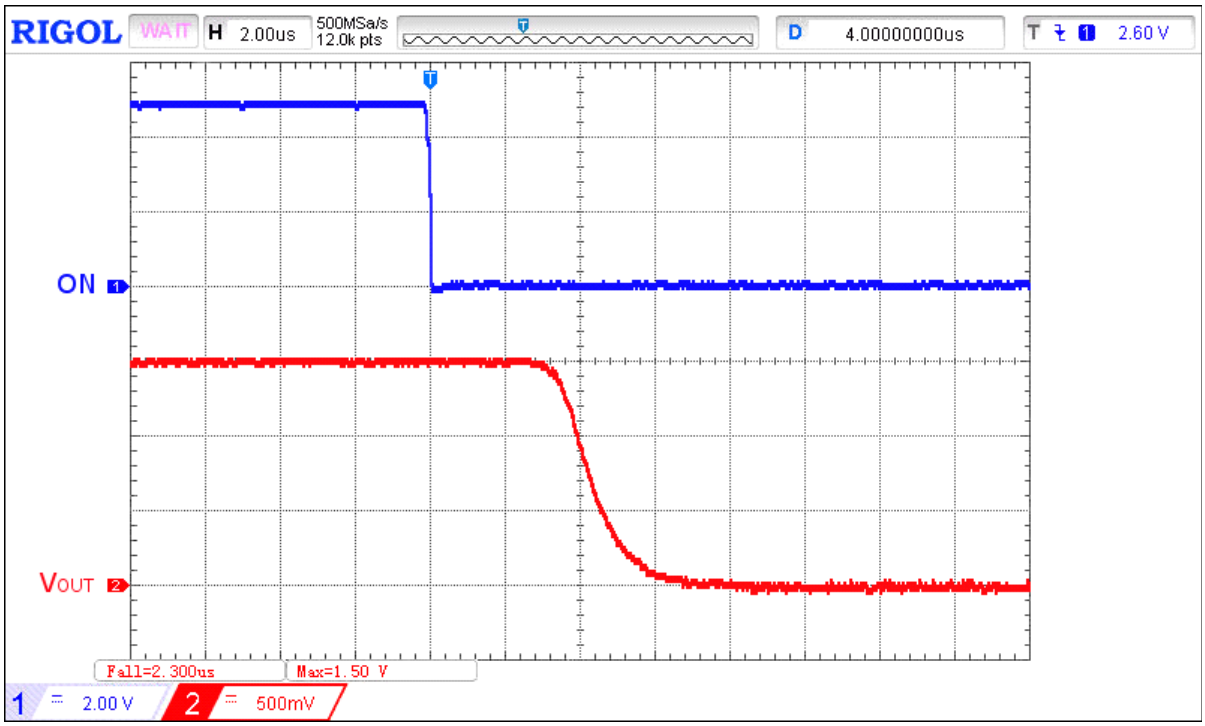



**Figure 9. Typical Turn OFF operation waveform for $V_{IN}$ = 1.5 V, $C_{LOAD}$ = 0.1 µF, $R_{LOAD}$ = 10 Ω**

## Monotonic Turn-on Waveforms

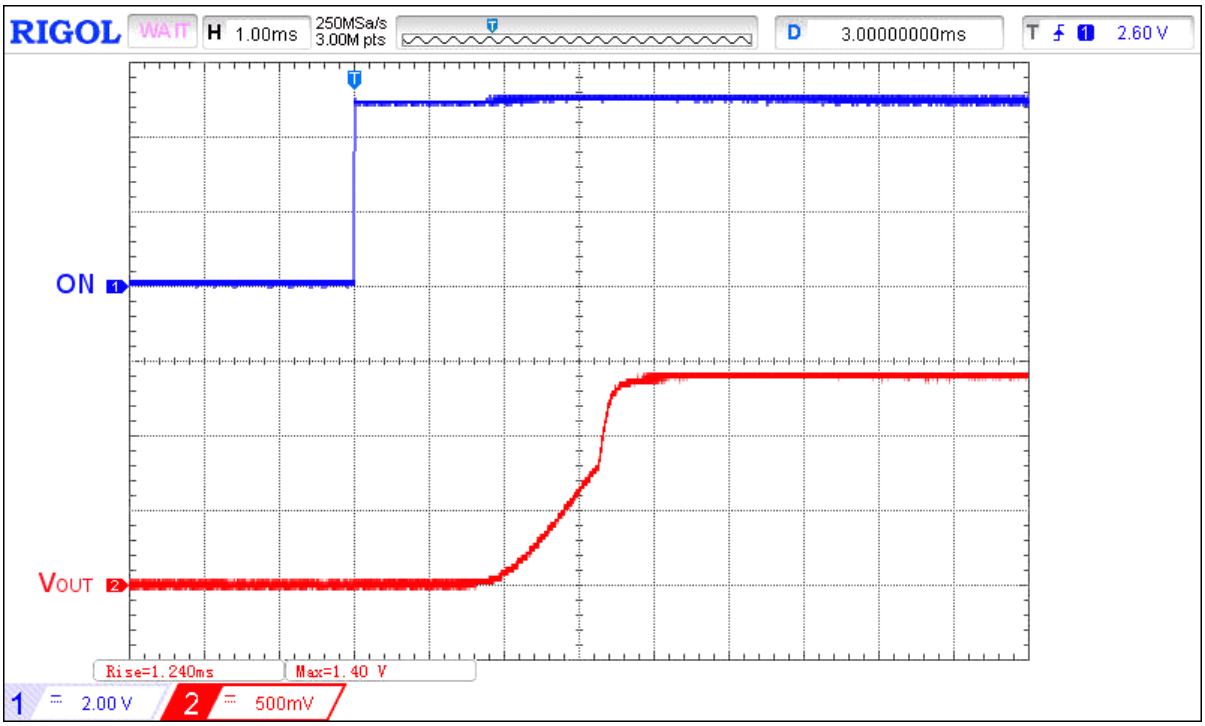



**Figure 10. Non-linear and monotonic turn ON operation waveform for $V_{IN}$ = 1.5 V, $C_{LOAD}$ = 0.1 µF, $R_{LOAD}$ = 1.5 Ω**

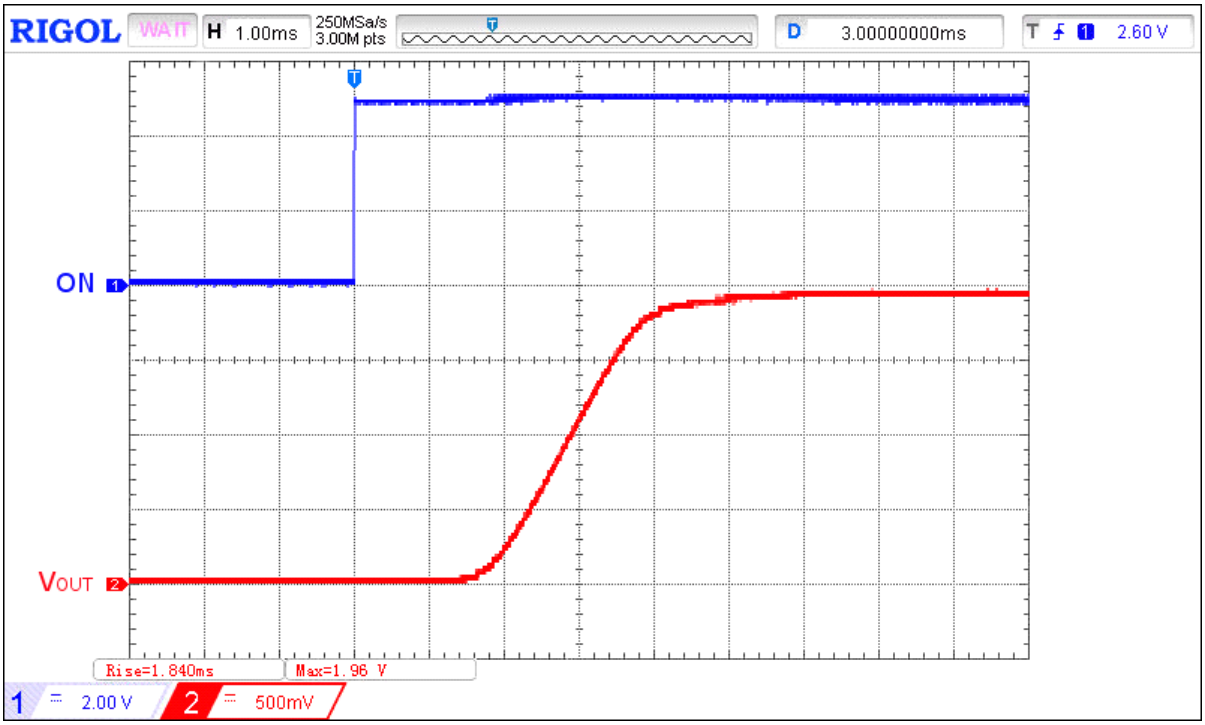



**Figure 11. Linear and monotonic turn ON operation waveform for $V_{IN}$ = 2 V, $C_{LOAD}$ = 0.1 µF, $R_{LOAD}$ = 2 Ω**

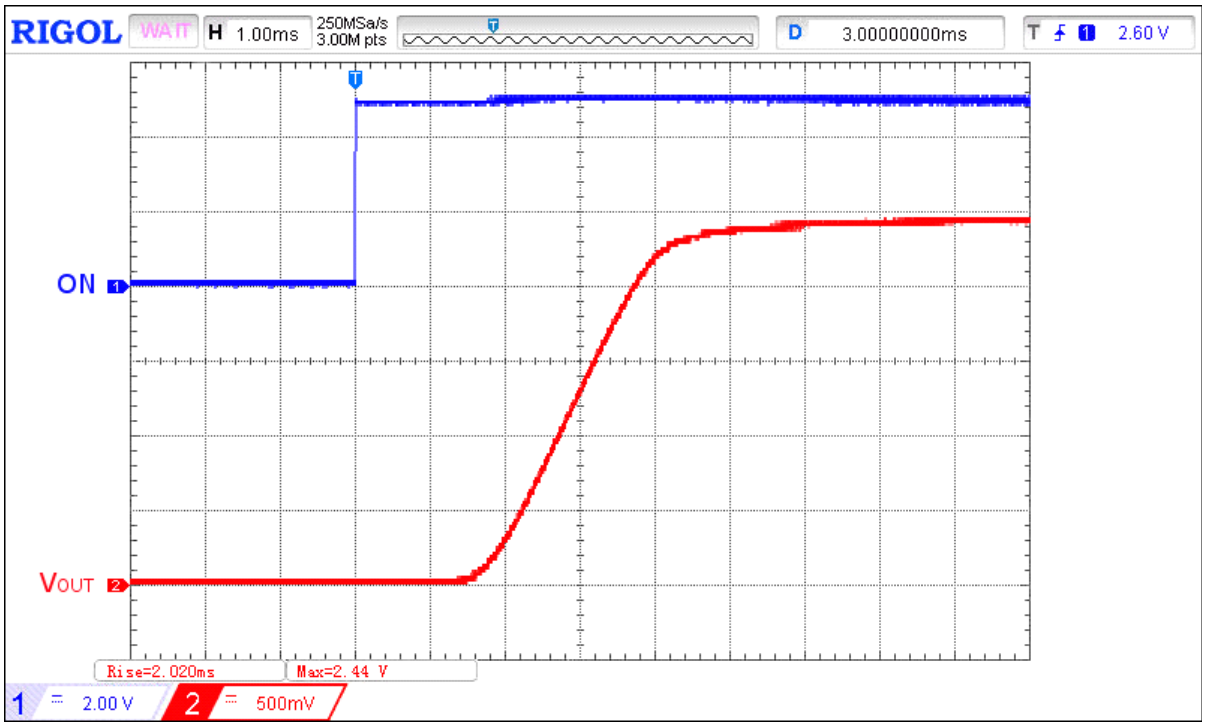
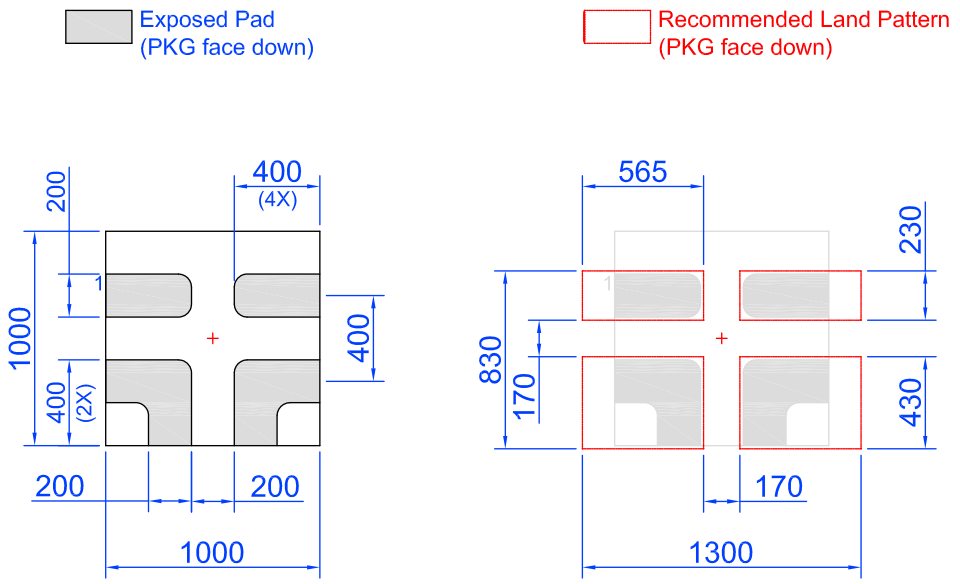



**Figure 12. Typical Turn ON operation waveform for $V_{IN}$ = 2.5 V, $C_{LOAD}$ = 0.1 µF, $R_{LOAD}$ = 2.2 Ω**

## SLG5NT1734V Power-Up/Power-Down Sequence Considerations

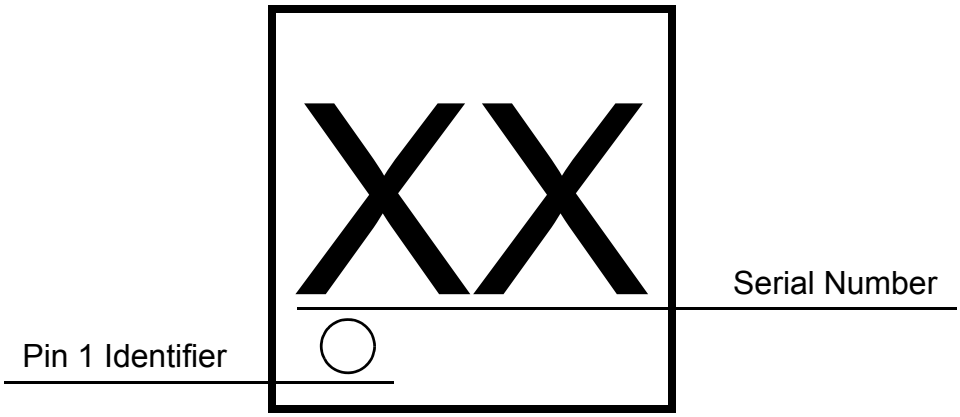
A nominal power-up sequence is to apply $V_{IN}$ and toggle the ON pin LOW-to-HIGH after $V_{IN}$ is at least 90% of its final value. A nominal power-down sequence is the power-up sequence in reverse order. If $V_{IN}$ ramp is too fast, a voltage glitch may appear on the output pin at VOUT. To prevent glitches at the output, it is recommended to connect at least 0.1uF capacitor from the VOUT pin to GND or to keep the $V_{IN}$ ramp time more than 2 ms.

## SLG5NT1734V Layout Suggestion



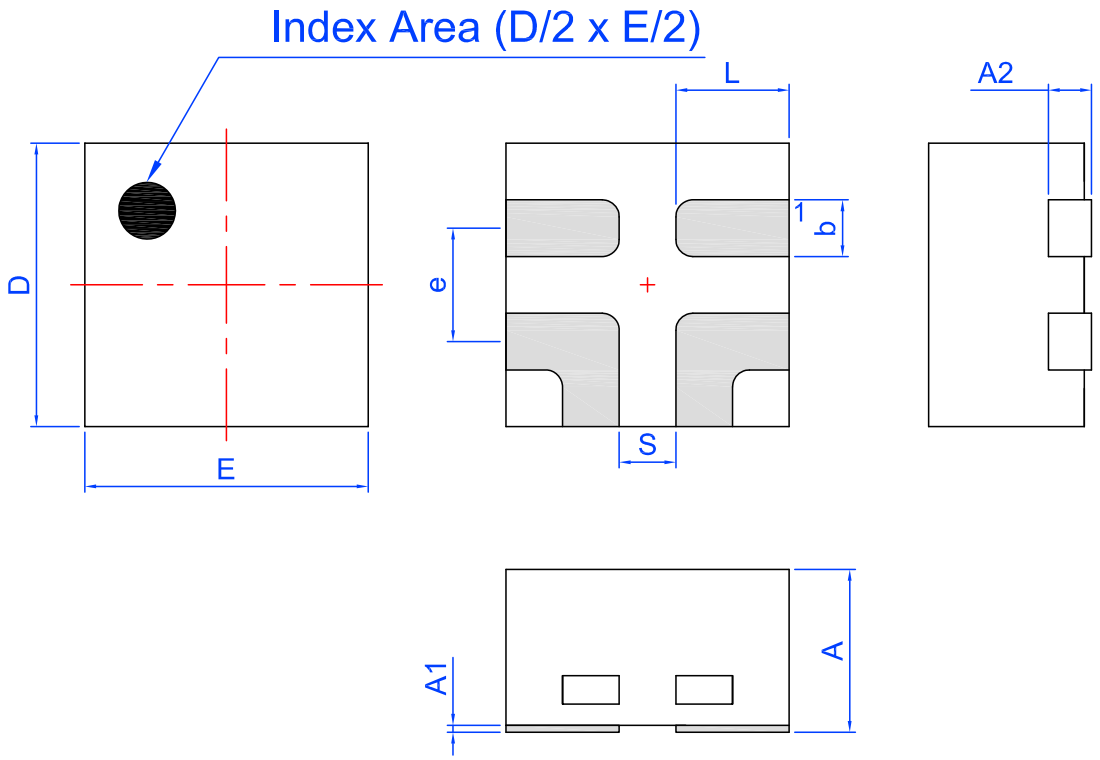

Note: All dimensions shown in micrometers (µm)

**Package Top Marking System Definition**



## Package Drawing and Dimensions

**4 Lead STDFN Package 1.0 x 1.0 mm**




Unit: mm

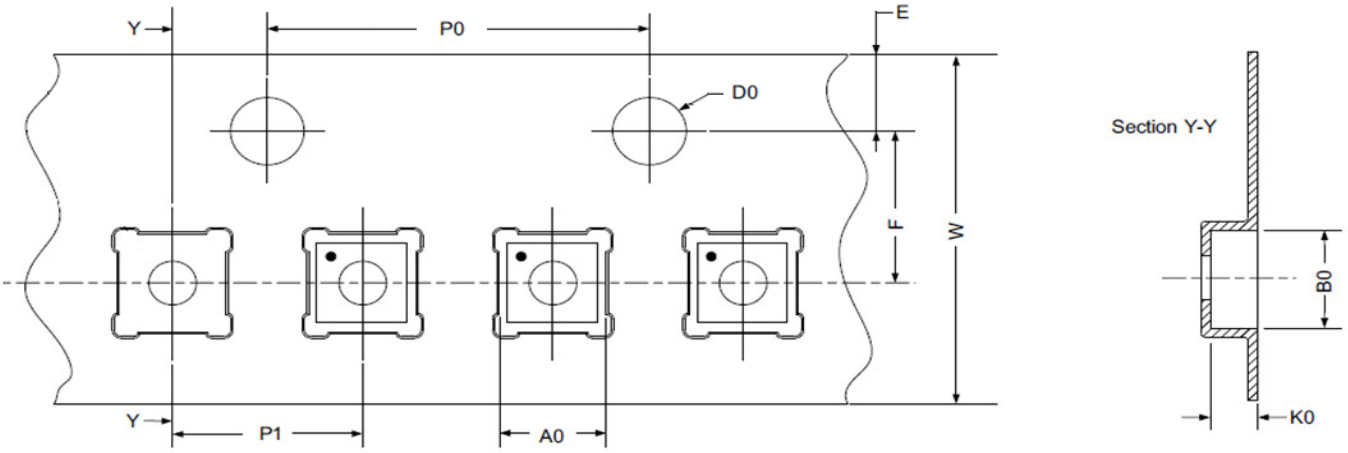
| Symbol | Min | Nom. | Max | Symbol | Min | Nom. | Max |
|---|---|---|---|---|---|---|---|
| A | 0.50 | 0.55 | 0.60 | D | 0.95 | 1.00 | 1.05 |
| A1 | 0.005 | - | 0.060 | E | 0.95 | 1.00 | 1.05 |
| A2 | 0.10 | 0.15 | 0.20 | L | 0.35 | 0.40 | 0.45 |
| b | 0.15 | 0.20 | 0.25 | S | 0.2 REF | | |
| e | 0.40 BSC | | | | | | |

## Tape and Reel Specifications

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| STDFN 4L 1x1mm 0.4P FC Green | 4 | 1.0 x 1.0 x 0.55 | 8000 | 8000 | 178 / 60 | 200 | 400 | 200 | 400 | 8 | 2 |

## Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|---|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| STDFN 4L 1x1mm 0.4P FC Green | 1.16 | 1.16 | 0.63 | 4 | 2 | 1.5 | 1.75 | 3.5 | 8 |




**Refer to EIA-481 specification**

## Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.55 $mm^3$ (nominal). More information can be found at www.jedec.org.

## Revision History

| Date | Version | Change |
|---|---|---|
| 8/7/2017 | 1.00 | Production Release |