Ultra-small Dual 40 mΩ, 1.0 A Integrated Power Switch with Discharge

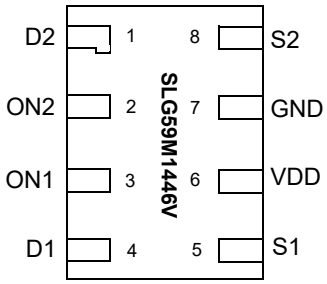
General Description

The SLG59M1446V is designed for power switching applications. The part comes with two 40 mΩ 1.0 A rated MOSFETs, each controlled by an ON control pin. Each MOSFET's ramp rate is adjustable depending on the input current level of the ON pin. The product is packaged in an ultra-small 1.6 x 1.0 mm package.

Features

- Two 40 mΩ 1.0 A MOSFETs
- Two integrated VGS Charge Pumps
- User selectable ramp rate with external resistor
- Protected by thermal shutdown
- Integrated Discharge Resistor
- Pb-Free / Halogen-Free / RoHS compliant
- STDFN 8L, 1.0 x 1.6 mm

Pin Configuration

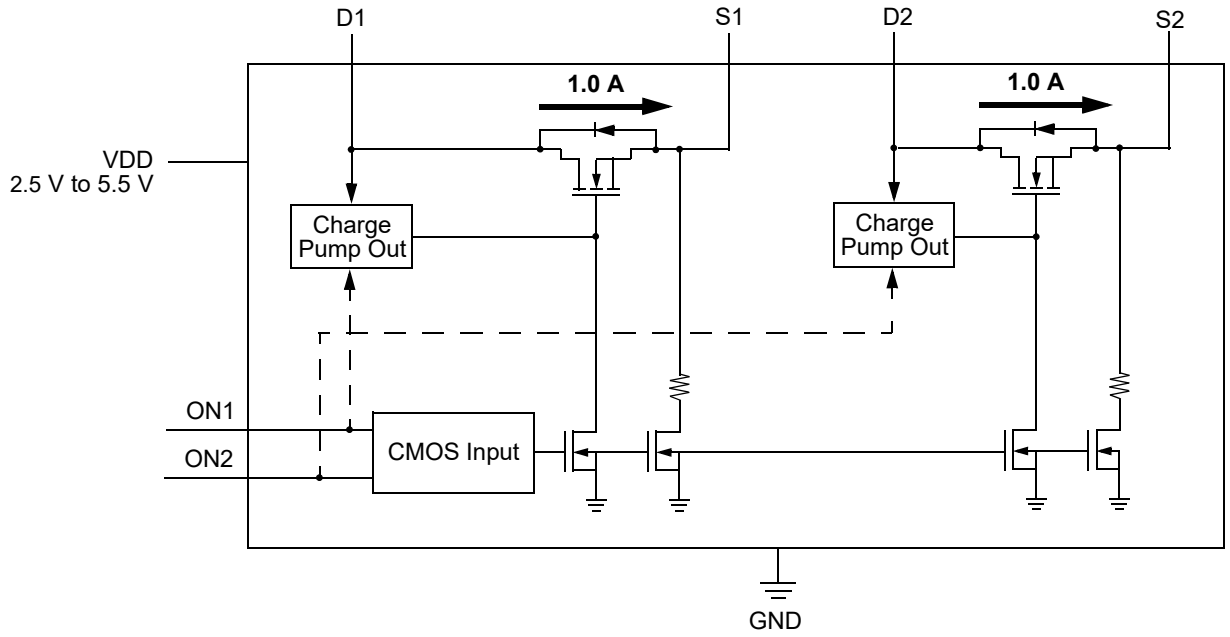


8-pin STDFN
(Top View)

Applications

- Power-Rail Switching:
  - Notebook/Laptop/Tablet PCs
  - Smartphones/Wireless Handsets
  - High-definition Digital Cameras
  - Set-top Boxes
- Point of Sales Pins
- GPS Navigation Devices

Block Diagram



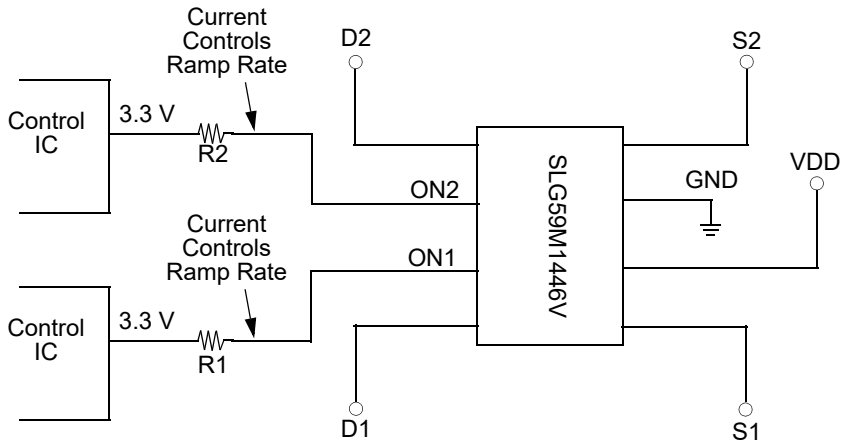
Pin Description

Pin #	Pin Name	Type	Pin Description
1	D2	MOSFET	Drain/Input terminal of Power MOSFET Channel 2. Connect a 10 µF (or larger) low ESR capacitor from this pin to GND. Capacitors used at D2 should be rated at 10 V or higher.
2	ON2	Input	A low-to-high transition on this pin closes the Channel 2 of power switch. ON is an asserted-HIGH, level-sensitive CMOS input with ON_V_{IL} < 0.3 V and ON_V_{IH_INI} > 1.2 V. Connect this pin to the output of a general-purpose output (GPO) from a microcontroller or other application processor. A resistor connected in series to ON2 signal sets the V_{S2} Slew Rate. Please read more information on Adjustable Slew Rate description.
3	ON1	Input	A low-to-high transition on this pin closes the Channel 1 of power switch. ON is an asserted-HIGH, level-sensitive CMOS input with ON_V_{IL} < 0.3 V and ON_V_{IH_INI} > 1.2 V. Connect this pin to the output of a general-purpose output (GPO) from a microcontroller or other application processor. A resistor connected in series to ON1 signal sets the V_{S1} Slew Rate. Please read more information on Adjustable Slew Rate description.
4	D1	MOSFET	Drain/Input terminal of Power MOSFET Channel 1. Connect a 10 µF (or larger) low ESR capacitor from this pin to GND. Capacitors used at D1 should be rated at 10 V or higher.
5	S1	MOSFET	Source/Output terminal of Power MOSFET Channel1. Connect a 10 µF (or larger) low ESR capacitor from this pin to GND. Capacitors used at S1 should be rated at 10 V or higher.
6	VDD	PWR	VDD supplies the power for the operation of the power switch and internal control circuitry where its range is 2.5 V ≤ V_{DD} ≤ 5.5 V. Bypass the VDD pin to GND with a 0.1 µF (or larger) capacitor.
7	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.
8	S2	MOSFET	Source/Output terminal of Power MOSFET Channel2. Connect a 10 µF (or larger) low ESR capacitor from this pin to GND. Capacitors used at S2 should be rated at 10 V or higher.

Ordering Information

Part Number	Type	Production Flow
SLG59M1446V	STDFN 8L	Industrial, -40 °C to 85 °C
SLG59M1446VTR	STDFN 8L (Tape and Reel)	Industrial, -40 °C to 85 °C

Application Diagram



Adjustable Ramp Rate vs. ON Pin Current (5.5 V, 25 °C)

ON Pin Current	$V_{S(SR)}$ (typ)
20 µA	0.56 V/ms
50 µA	1.34 V/ms
100 µA	2.53 V/ms
150 µA	3.71 V/ms
200 µA	4.68 V/ms
250 µA	5.63 V/ms

Adjustable Slew Rate (ON2 Pin 2 and ON1 Pin3)

SLG59M1446V has a built in configurable slew control feature. The configurable slew control uses current detection method on ON1/ON2. When ON voltage rises above $ON\_V_{IH\_INI}$ (1.2 V typical), the slew control circuit will measure the current flowing into ON1/ON2. Based on the current flowing into ON1/ON2, different slew rates will be selected by the internal control circuit. See ON Pin Curent vs. $V_{S(SR)}$ table. The slew rate is configurable by selecting a different R1/R2 resistor value as shown on application diagram. Calculating the R1/R2 value depends on both the desired slew rate, and the V_{OH} level of the device driving the ON1/ON2 pin.

ON Pin Current = ($GPIO\_V_{OH}$ – ON_V_{REF} (1.05 V typical)) / R

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage		--	--	6	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	1000	--	--	V
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Thermal Resistance,	1 x 1.6mm STDFN; Determined using 1 in^2, 1 oz. copper pads under each Dx and Sx terminal and FR4 pcb material	--	72	--	°C/W
W_{DIS}	Package Power Dissipation		--	--	0.4	W
MOSFET IDS_{PK}	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	--	--	1.5	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	Pin 6	2.5	--	5.5	V
V_{D1}	Power Switch Input Voltage of Channel 1	Pin 4	0.85	--	V_{DD}	V
V_{D2}	Power Switch Input Voltage of Channel 2	Pin 1	0.85	--	V_{DD}	V
I_{DD}	Power Supply Current (PIN 6)	when OFF	--	0.1	1	µA
		when ON, No load	--	35	50	µA
$RDS_{ON[1,2]}$	ON Resistance	T_A = 25 °C, I_{DS} = 100 mA	--	40	50	mΩ
		T_A = 70 °C, I_{DS} = 100 mA	--	50	55	mΩ
		T_A = 85 °C, I_{DS} = 100 mA	--	55	65	mΩ
MOSFET IDS	Current from D[1,2] to S[1,2]	Continuous	--	--	1.0	A
T_{ON_Delay}	ON Delay Time	50% ON to $V_{S[1,2]}$ Ramp Start; ON Pin Current (PIN2, PIN3) = 20 µA; V_{DD} = $V_{D[1,2]}$ = 5 V; C_{LOAD} = 10 µF; R_{LOAD} = 20 Ω	--	2.4	4.0	ms
T_{Total_ON}	Total Turn On Time	50% ON to 90% $V_{S[1,2]}$	Configurable[1]			ms
		Example: ON Pin Current (PIN2, PIN3) = 20 µA; V_{DD} = $V_{D[1,2]}$ = 5 V; C_{LOAD} = 10 µF; R_{LOAD} = 20 Ω	--	11.7	--	ms
$V_{S(SR)}$	$V_{S[1,2]}$ Slew Rate	10% $V_{S[1,2]}$ to 90% $V_{S[1,2]}$	Configurable[1]			V/ms
		Example: ON Pin Current (PIN2, PIN3) = 20 µA; V_{DD} = $V_{D[1,2]}$ = 5 V; C_{LOAD} = 10 µF; R_{LOAD} = 20 Ω	--	0.56	--	V/ms
$R_{DISCHRG}$	Discharge Resistance	V_{DD} = 2.5 V to 5.5 V; $V_{S[1,2]}$ = 0.4 V Input bias	100	150	300	Ω

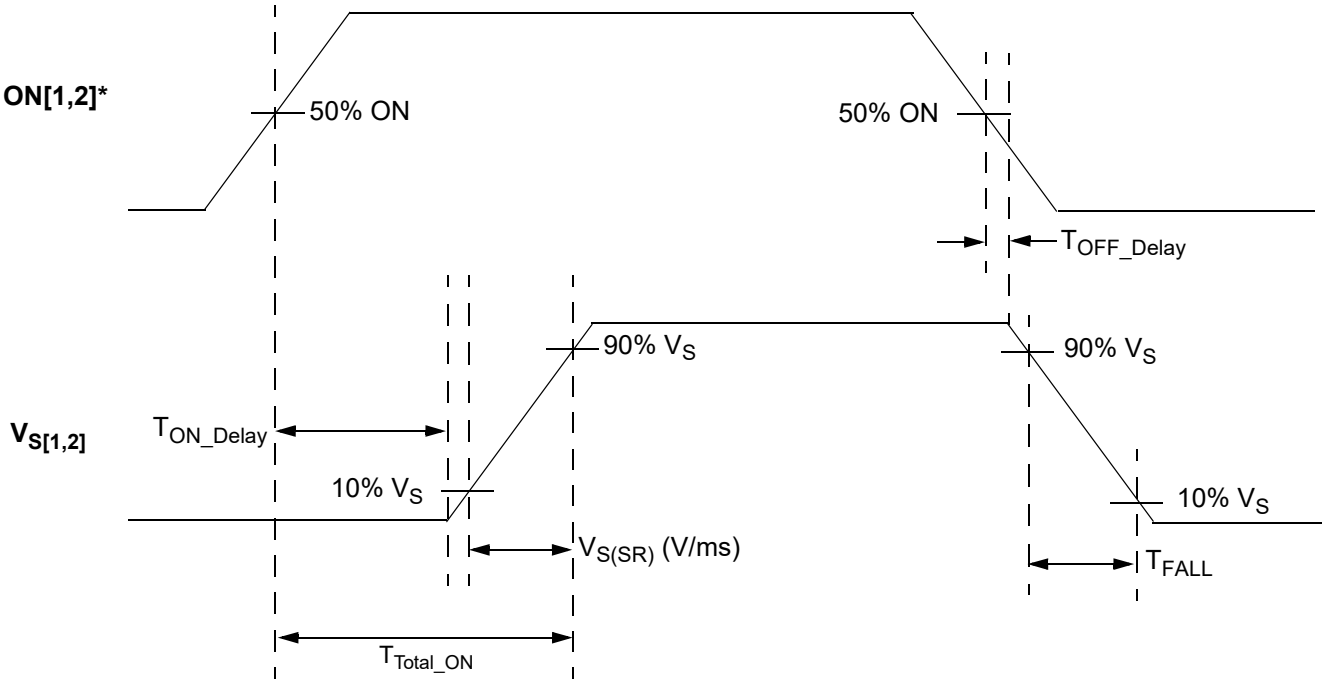
Electrical Characteristics (continued)

T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from S[1,2] to GND	--	--	100	µF
ON_V_{REF}	ON Pin Reference Voltage [2]		0.99	1.05	1.10	V
ON_V_{IH_INI}	Initial Turn On Voltage	Internal Charge Pump ON	1.2	--	V_{DD}	V
ON_V_{IL}	Low Input Voltage on ON pin	Internal Charge Pump OFF	-0.3	0	0.3	V
ON_R	Input Impedance on ON pin		100	--	--	MΩ
$THERM_{ON}$	Thermal shutoff turn-on temperature		--	125	--	°C
$THERM_{OFF}$	Thermal shutoff turn-off temperature		--	100	--	°C
$THERM_{TIME}$	Thermal shutoff time		--	--	1	ms
T_{OFF_Delay}	OFF Delay Time	50% ON to $V_{S[1,2]}$ Fall Start; $V_{D[1,2]}$ = 5 V; R_{LOAD} = 20 Ω; no C_{LOAD}	--	55	70	µs
T_{FALL}	$V_{S[1,2]}$ Fall Time	90% $V_{S[1,2]}$ to 10% $V_{S[1,2]}$; $V_{D[1,2]}$ = 5 V; R_{LOAD} = 20 Ω; no C_{LOAD}	--	32	--	µs

Notes:
1. Refer to table for configuration details.
2. Voltage before ON pin resistor needs to be higher than 1.2 V to generate required I_{ON}

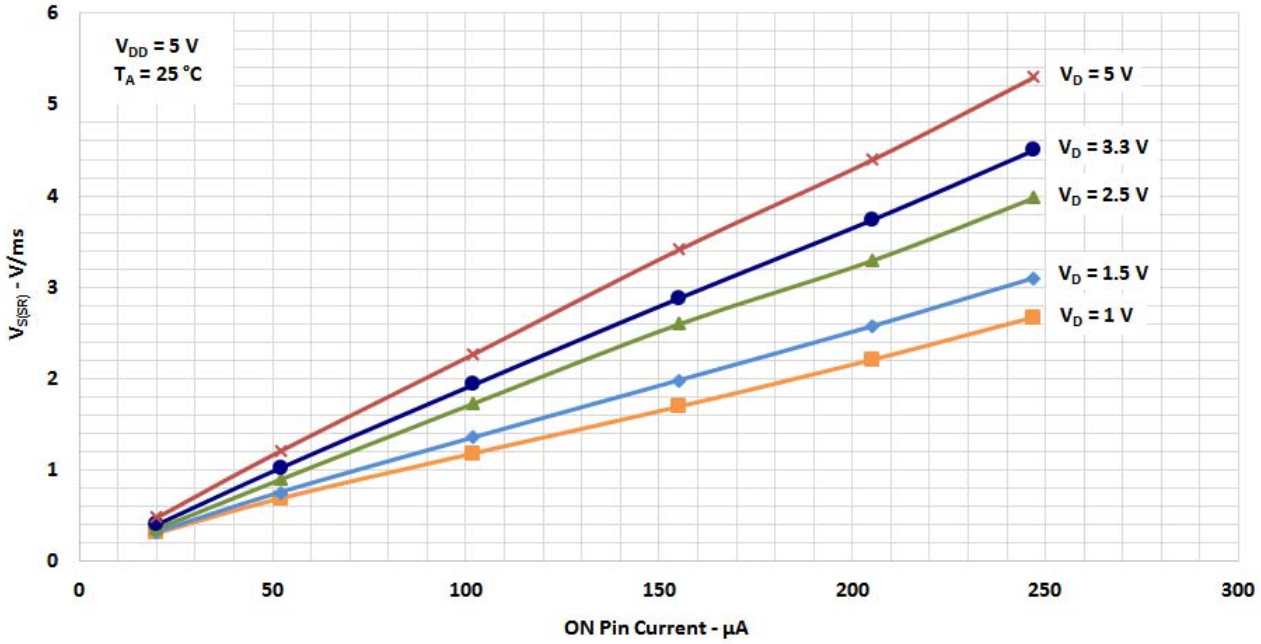
T_{ON_Delay}, $V_{S(SR)}$, and T_{Total_ON} Timing Details



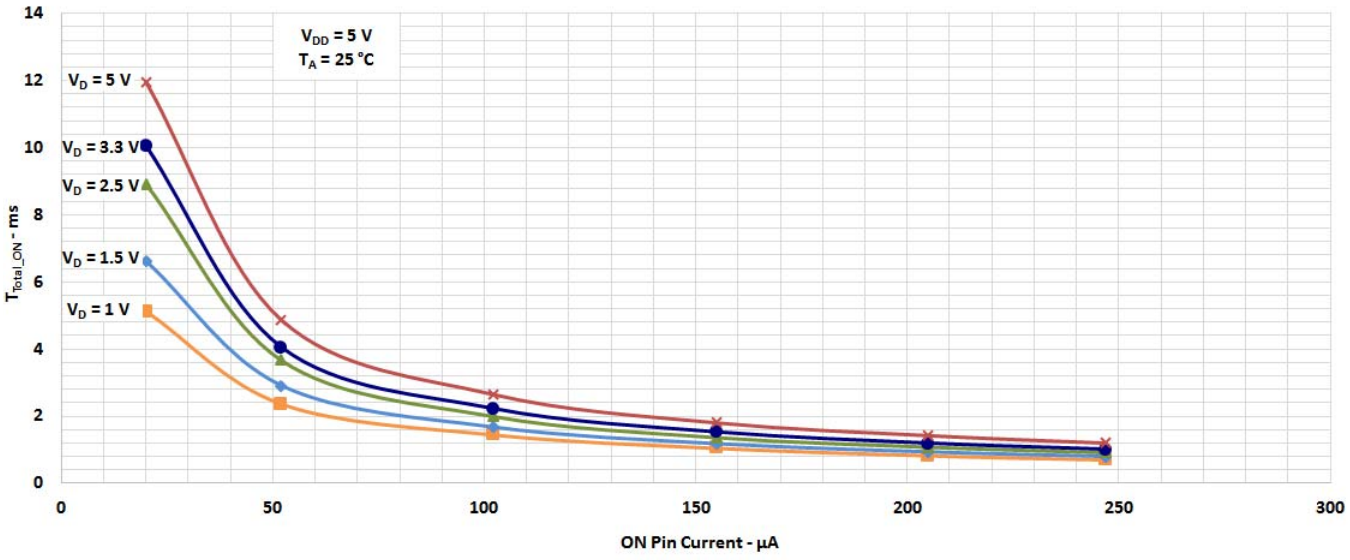
*Rise and Fall Times of the ON Signal are 100 ns

Typical Performance Characteristics

Slew Rate vs. ON Current



T_{Total_ON} vs. ON Current



Power Dissipation

The junction temperature of the SLG59M1446V depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the RDS_{ON}-generated voltage drop across each power MOSFET. While the primary contributor to the increase in the junction temperature of the SLG59M1446V is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = (RDS_{ON1} \times I_{DS1}^2) + (RDS_{ON2} \times I_{DS2}^2)$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

$RDS_{ON[1,2]}$ = Channel 1 and Channel 2 Power MOSFET ON resistance, in Ohms (Ω), respectively

$I_{DS[1,2]}$ = Channel 1 and Channel 2 Output current, in Amps (A), respectively

and

$$T_J = PD_{TOTAL} \times \theta_{JA} + T_A$$

where:

T_J = Die junction temperature, in Celsius degrees (°C)

θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on pcb layout

T_A = Ambient temperature, in Celsius degrees (°C)

In nominal operating mode, the SLG59M1446V's power dissipation can also be calculated by taking into account the voltage drop across each switch (V_{Dx} - V_{Sx}) and the magnitude of that channel's output current (I_{DSx}):

$$PD_{TOTAL} = [(V_{D1}-V_{S1}) \times I_{DS1}] + [(V_{D2}-V_{S2}) \times I_{DS2}] \text{ or}$$

$$PD_{TOTAL} = [(V_{D1} – (R_{LOAD1} \times I_{DS1})) \times I_{DS1}] + [(V_{D2} – (R_{LOAD2} \times I_{DS2})) \times I_{DS2}]$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

$V_{D[1,2]}$ = Channel 1 and Channel 2 Input Voltage, in Volts (V), respectively

$R_{LOAD[1,2]}$ = Channel 1 and Channel 2 Output Load Resistance, in Ohms (Ω), respectively

$I_{DS[1,2]}$ = Channel 1 and Channel 2 output current, in Amps (A), respectively

$V_{S[1,2]}$ = Channel 1 and Channel 2 output voltage, or $R_{LOAD[1,2]} \times I_{DS[1,2]}$, respectively

Layout Guidelines:

1. The VDD pin needs a 0.1 µF external capacitor to smooth pulses from the power supply. Locate this capacitor as close as possible to the SLG59M1446V's PIN6.

2. Since the D1, D2, S1 and S2 pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 1, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

3. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59M1446V's D1, D2, S1 and S2 pins;

4. The GND pin should be connected to system analog or power ground plane.

5. 2 oz. copper is recommended for high current operation.

SLG59M1446V Evaluation Board:

A GFET3 Evaluation Board for SLG59M1446V is designed according to the statements above and is illustrated on Figure 1. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

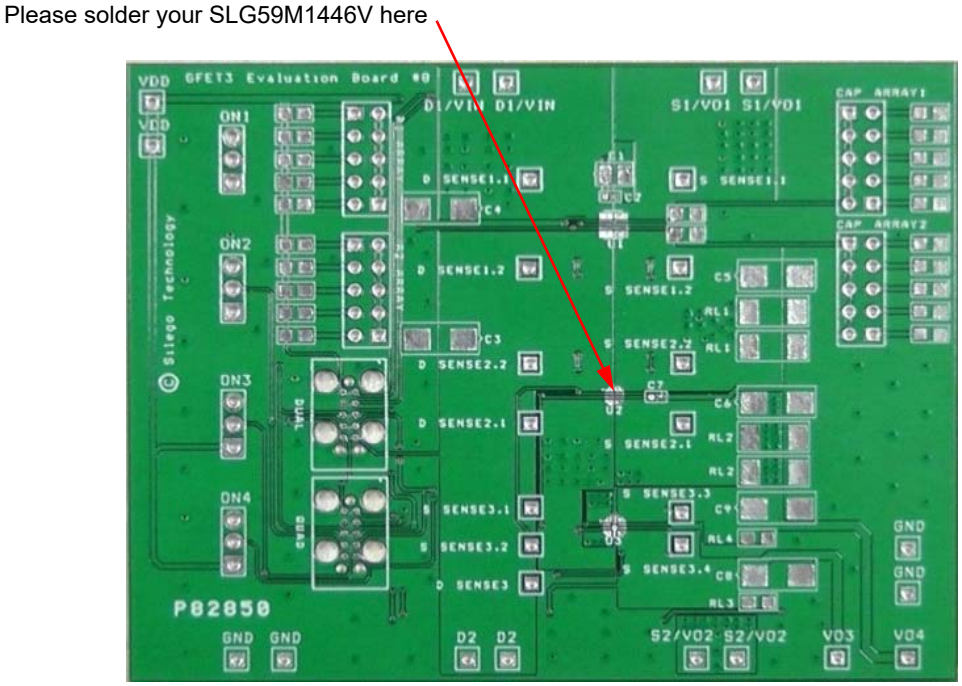


Figure 1. SLG59M1446V Evaluation Board.

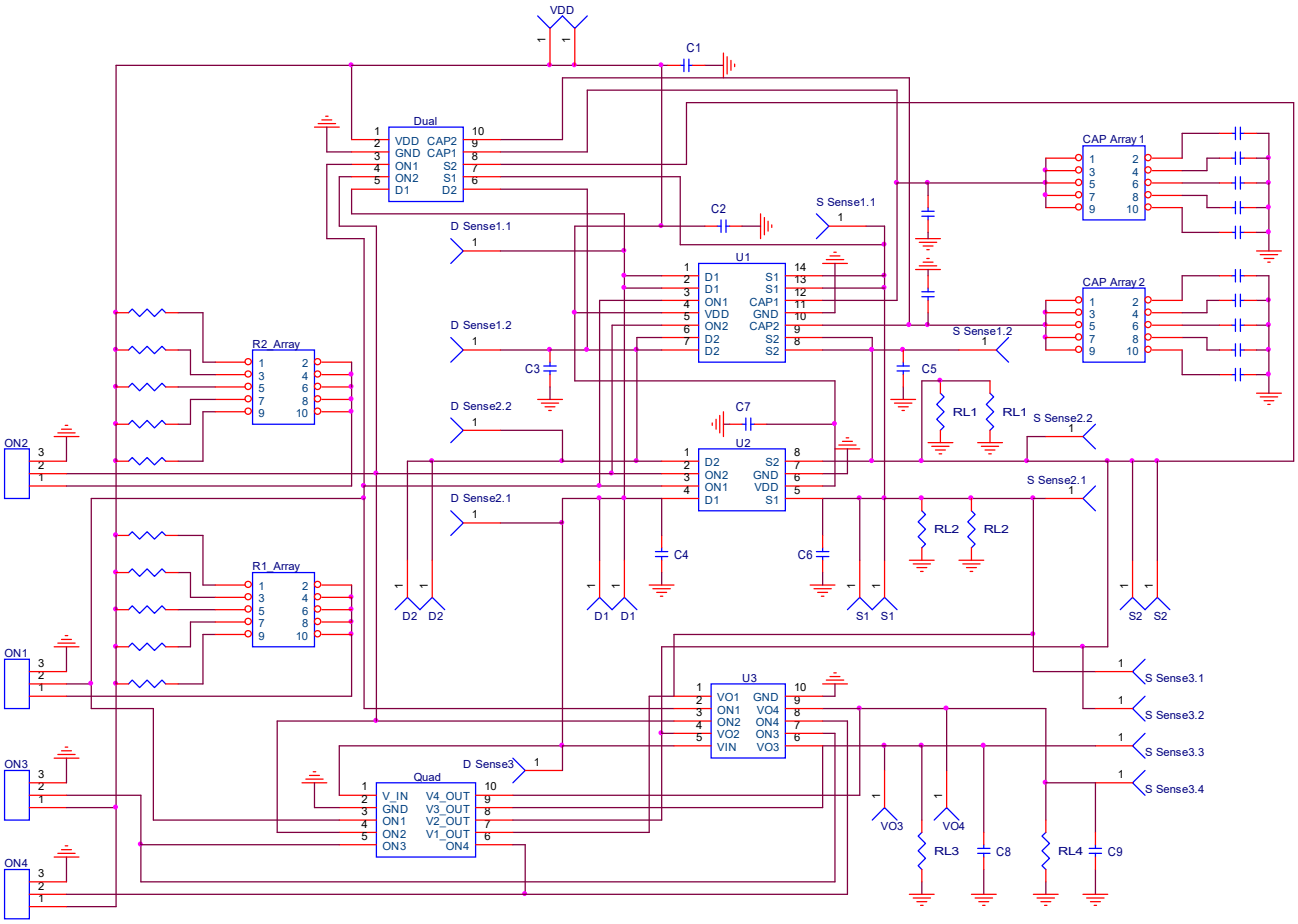


Figure 2. SLG59M1446V Evaluation Board Connection Circuit.

Basic Test Setup and Connections

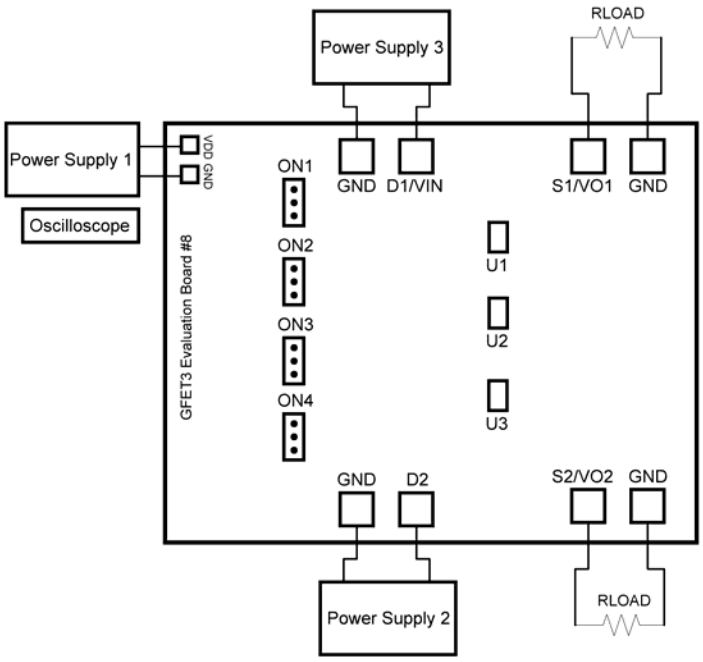


Figure 3. Typical connections for GFET3 Evaluation.

EVB Configuration

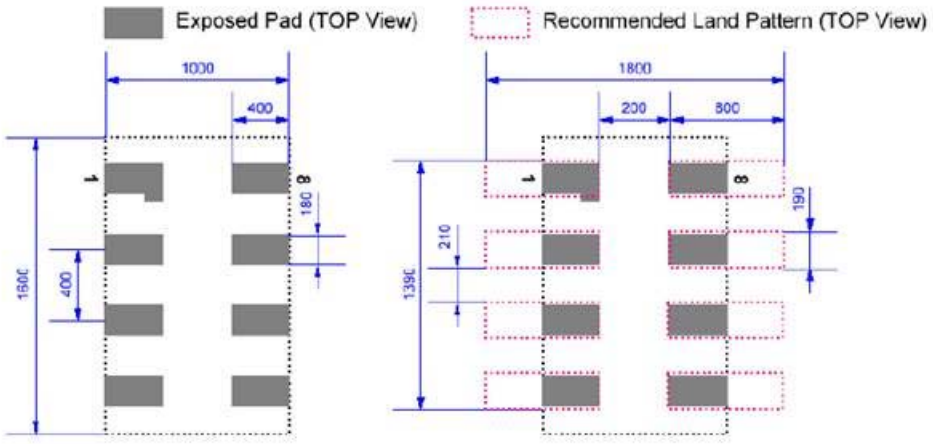
1.Connect oscilloscope probes to D1/VIN, D2, S1/VO1, S2/VO2, ON1, ON2 etc.;

2.Turn on Power Supply 1 and set desired V_{DD} from 2.5 V…5.5 V range;

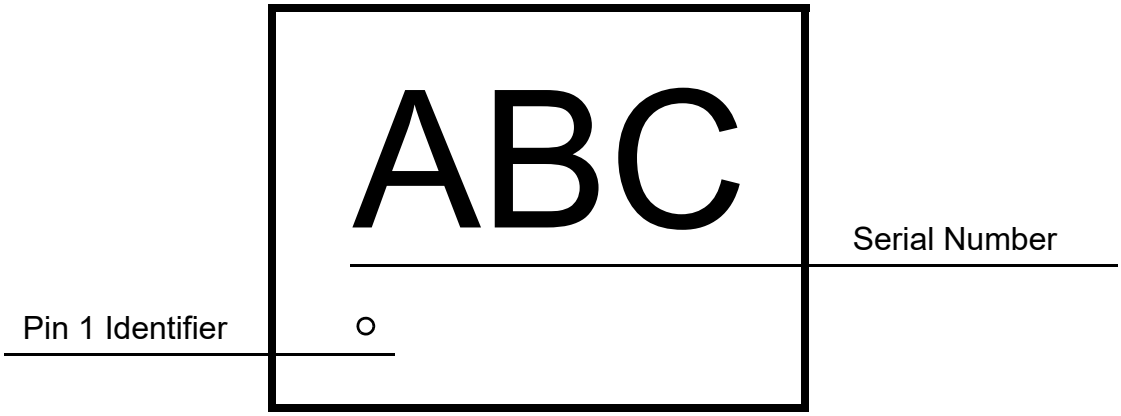
3.Turn on Power Supply 2, 3 and set desired $V_{D[1,2]}$ from 0.85 V…V_{DD} range;

4.Toggle the ON[1,2] signal High or Low to observe SLG59M1446V operation.

SLG59M1446V Layout Suggestion



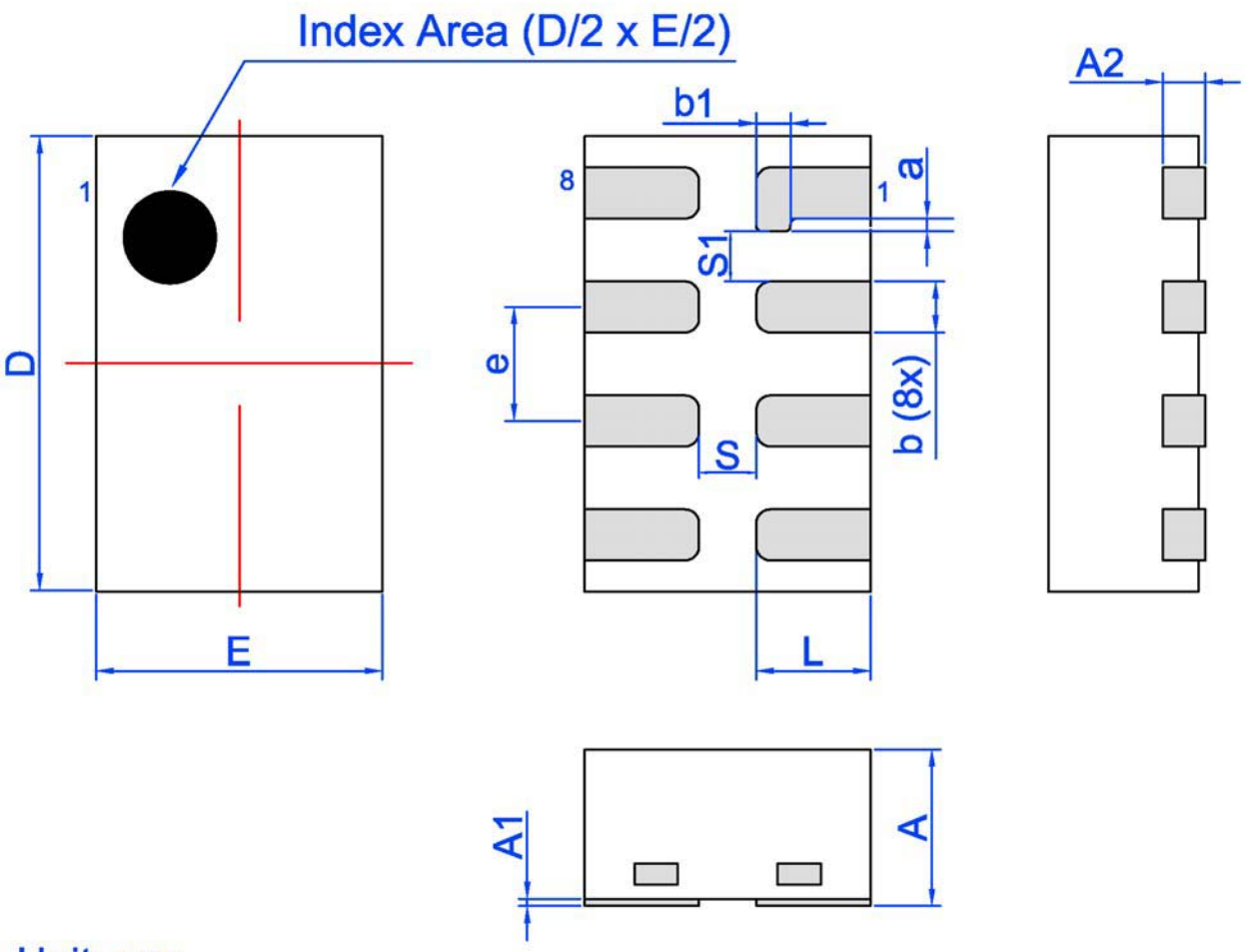
Package Top Marking System Definition



ABC - 3 alphanumeric Part Serial Number
where A, B, or C can be A-Z and 0-9

Package Drawing and Dimensions

8 Lead STDFN Package 1.0 x 1.6 mm



Unit: mm

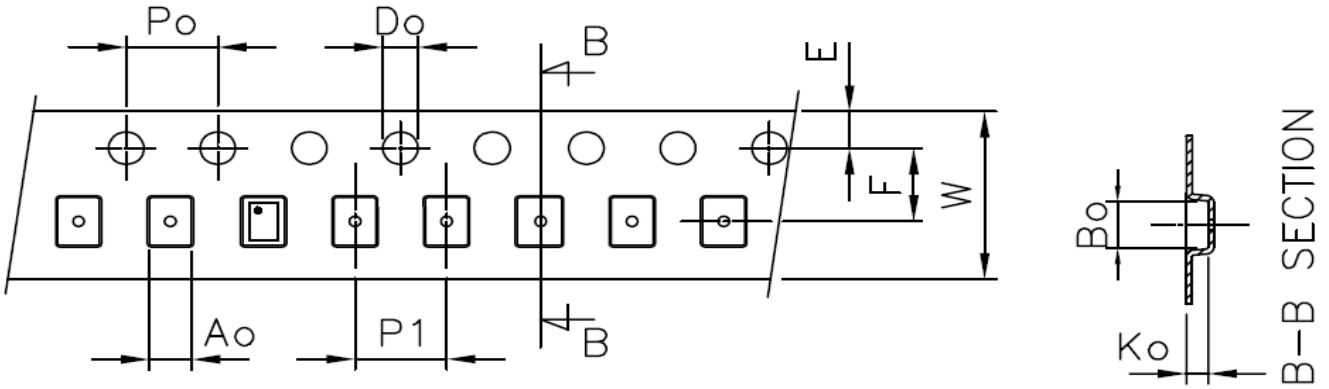
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.13	0.18	0.23	S	0.2 REF		
b1	0.17	0.19	0.20	a	0.04	0.05	0.06
e	0.40 BSC			S1	0.175 REF		

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STDFN 8L 1x1.6mm 0.4P Green	8	1.0 x 1.6 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 8L 1x1.6mm 0.4P Green	1.12	1.72	0.7	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.88 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
9/13/2019	1.05	Updated Pin Descriptions Updated style and formatting Updated Charts Added Power Dissipation Updated POD Fixed typos
12/4/2015	1.04	Updated Block Diagram
11/20/2015	1.03	Added ESD_{CDM}, MSL, and θ_{JA} specs