# Errata Sheet

SLG46855

ISSUE 1: Incorrect I²C Reads of the 8-bit Counter Registers
Functional Blocks Affected: CNT2/DLY2 and CNT4/DLY4

Description:

Asynchronous interaction between the CNT/DLY clock input and the I²C latch signal (generated by an I²C read command of the CNT/DLY block's count value) can result in an incorrect I²C data read. The CNT/DLY block will count accurately, but the count value transferred into the block's I²C read register might be loaded incompletely if the I²C latch signal and the clock input occur at about the same time.

The example data capture below shows ten periodic I²C reads of CNT2/DLY2 configured to count down at about 16 clocks per read. The sixth read sample erroneously shows a value greater than that of the fifth. The seventh sample reads as if the previous I²C error never occurred - the difference from the fifth sample (176) to the seventh (143) is 33 clocks or 16 clocks + 17 clocks as expected.

Channel 1 (yellow/top line) – PIN#2 (CNT2/DLY2 Out)
Channel 2 (light blue/2nd line) – PIN#1 (I²C Read Triggers)
Channel 3 (magenta /3rd line) – PIN#8 (I²C SCL)
Channel 3 (dark blue /4th line) – PIN#9 (I²C SDA)
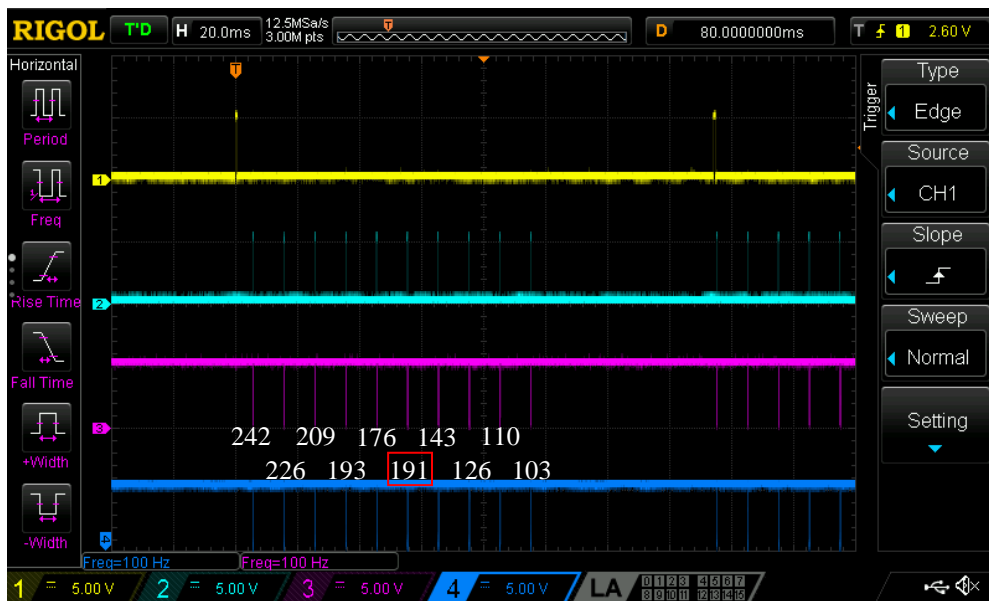
Workaround:

If the possibility of incorrect I²C data reads can't be accommodated for by external software checks, one can guarantee proper operation by stopping the CNT/DLY block's clock during I²C reads through one of the following methods: by disabling the oscillator block, by reconfiguring the CNT/DLY block's clock source, or by gating an external clock using a LUT (Look-up Table) in the signal matrix. After disabling the CNT/DLY block's clock, the count registers can be read without error. Please note that this workaround will add the I²C read and processing time to the counter's overall clock period.

The best workaround depends on the resource constraints of the application. If the oscillator block doesn't clock other logic elements within the design, a matrix output can be used to manually power down the oscillators for the I²C read. When the CNT/DLY block's clock source is routed internally from the oscillator block, I²C commands can temporarily reconfigure the CNT/DLY block's clock source registers to select "Ext. CLK. (From Matrix)." This action will disable the clock by connecting it to ground. If the CNT/DLY block is clocked from the signal matrix, a LUT can be used to gate the clock during an I²C read.

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## ISSUE 2: Noise Coupling from VREF0 to Low-Power Bandgap
Functional Blocks Affected: All ACMPs

Description:

There is some noise coupling from the VREFs of high-speed ACMPs to the low-power bandgap (BG) while the high-speed ACMPs VREF is turning on and off.

Workaround:

There is no issue with manually powering up the low-speed ACMPs. If you are manually powering up the high-speed ACMPs via the "PWR UP" connector, you should add a 1 ms delay to the output of all of the ACMPs used in the design.

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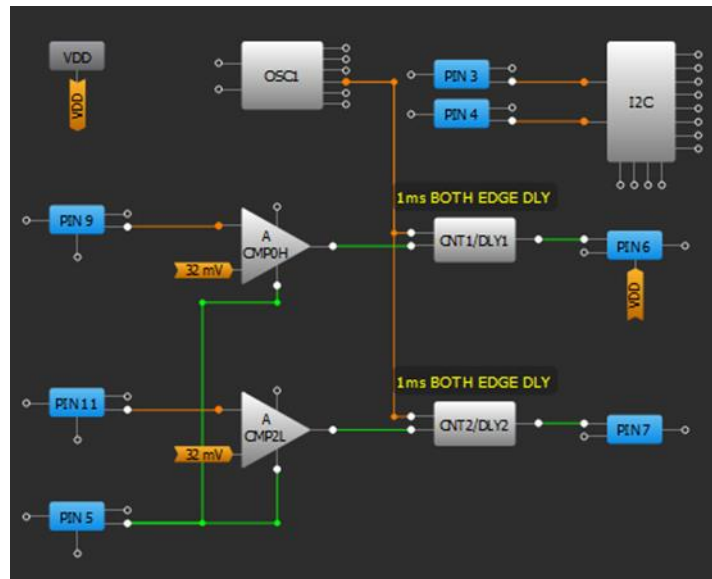
ISSUE 3: Unstable VREF Output Buffer
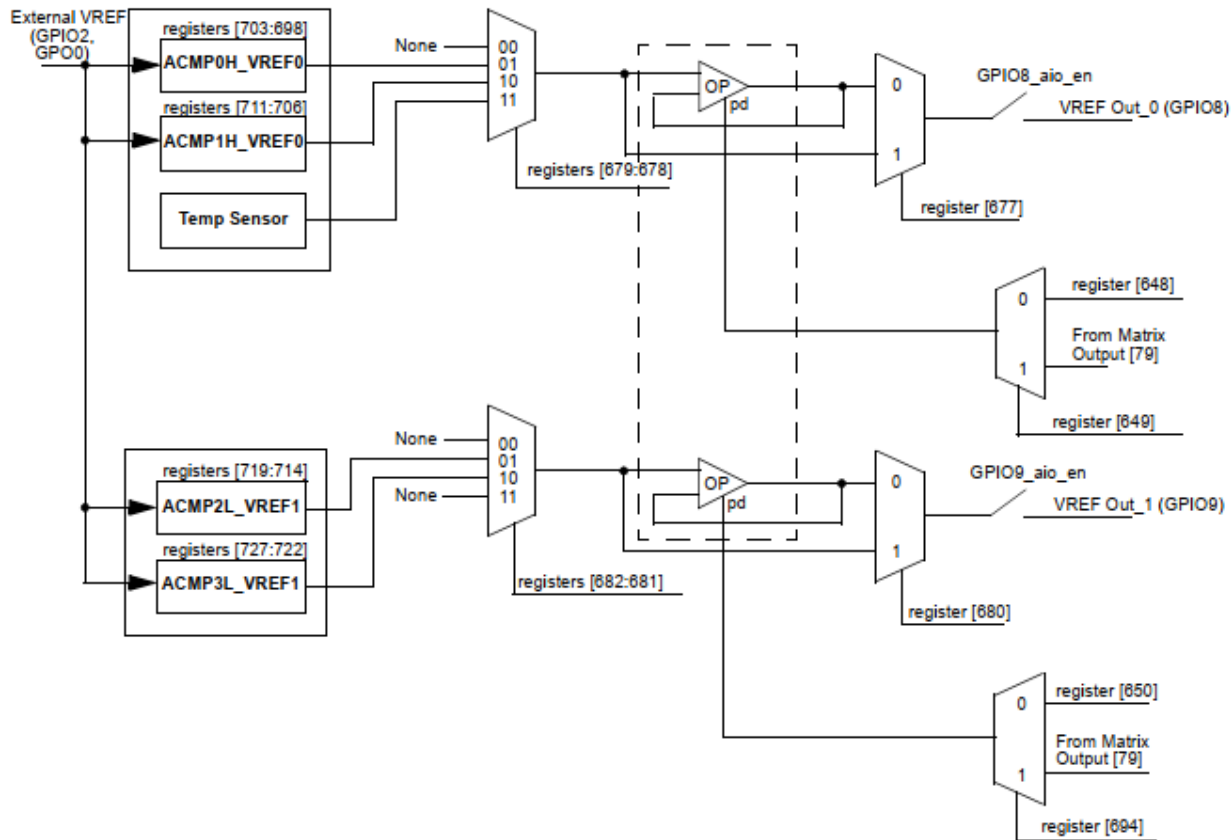## Functional Blocks Affected: Both VREF Output

Description:

For systems where V_{DD} = 2.5 V, the VREF output buffer will be unstable if the output voltage is around $0.5xV_{DD}$.

Workaround:

For a system where V_{DD} = 2.5 V, bypass the buffer if the output voltage of the VREF buffer is within $(0.5xV_{DD})$ ± 0.4. Check the VREF section of the device datasheet to see which registers need to be modified.

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ISSUE 4: Incorrect Data Write
Functional Blocks Affected: I²C

Description:

When performing a masked I²C write, unchanged bits in the 8-bit I²C bus may be coupled to the changed bits due to the large coupling capacitor between the I²C bus bits, leading to incorrect data being written.

Workaround:

There is no workaround, but this will be fixed in the next silicon revision.

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ISSUE 5: Extra 300 µA Current Consumption when using SCL and SDA Pins as GPIO
Functional Blocks Affected: GPIO0, GPIO1

Description:

When using the I²C SCL and SDA pins as GPIO outputs, there is an internal block that causes about 300 µA of current consumption. This does not appear when the I²C pins are used as either digital input pins or as I²C pins.

Workaround:

There is no workaround. It is not recommended to use these pins as Digital Outputs.

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ISSUE 6: Leakage from ACMP IN+ to Analog Input Pins
Functional Blocks Affected: GPIO4/5/6/7, ACMP0/1H, ACMP2/3L
Description:

When configured in "Analog IO" mode, GPIO4/5/6/7 can experience abnormal leakage behavior. This behavior occurs when multiple input sources are simultaneously connected to the ACMP IN+ port. Each of the 4 ACMPs has an input MUX which selects the IN+ source for the comparator. The MUX options are shown in the table below.

Table 1: ACMP Input Options

ACMP IN+ MUX Options	
ACMP0H	GPIO4 Buffered GPIO4 VDD
ACMP1H	GPIO5 Buffered GPIO5 ACMP0H IN+ source
ACMP2L	GPIO6 ACMP0H IN+ source ACMP1H IN+ source
ACMP3L	GPIO7 ACMP2L IN+ source VREF0 output

In the GreenPAK Designer, the input source is selected by the IN+ source dropdown within the ACMP's properties window. When an input source is selected and the ACMP is enabled, an analog switch connects the source to the ACMP's IN+ port. If multiple sources are connected to the ACMP's IN+ port, there will be leakage between the sources.

The GPIOs shown above can be repurposed as Digital IOs if the ACMPs are disabled or if another input source is selected for the ACMP by the IN+ input MUX. Whenever a GPIO input mode is configured as an "Analog IO" in accordance with the register definition below, the GPIO will be connected to the ACMP's IN+ port through an internal switch. This can create a leakage scenario if the ACMP is enabled and connected to another input source.

Table 2: GPIO Input Mode Configurations

Byte	Register Bit	Signal Function	Register Bit Definition
GPIO4			
0x66	821	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
	822		
GPIO5			
0x67	829	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
	830		
GPIO6			
0x68	836	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
	837		
GPIO7			
0x69	843	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
	844		

There are 3 standard GPIO settings that use the "Analog IO" configuration: Analog input/output, Digital input/output (with "Input mode" set to Analog input), and Digital output (with "Output mode" set to 1/2/4x 3-State Output). The first setting is reserved for use with the ACMP, but the other two settings use the "Analog IO" configuration as a high-impedance input. It is important to note that these input modes won't be high impedance if the ACMP is enabled and connected to another input source. When two signals are connected to the ACMP's IN+ source, the voltage level at the ACMP's input depends upon the drive strength of the competing sources.

Figure below shows the GreenPAK configured with GPIO4 as a Digital IO with a 1MΩ pull down resistor. Since the OE pin is connected to 0V, this pin is acting as an "Analog IO." As seen in Table 1 above, GPIO4 and VDD are both input options for ACMP0H. In this example, GPI0 is being used as a digital input to enable and disable the ACMP.
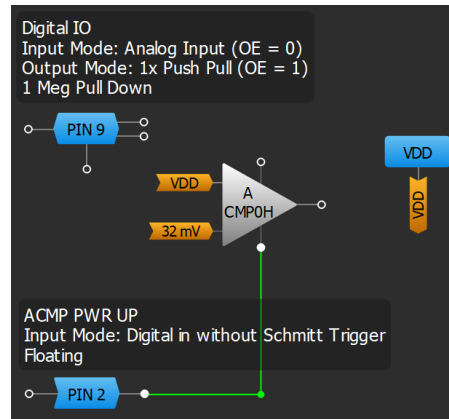

GreenPAK Input Structure Test Schematic

Figure below shows that GPIO4 in analog input mode is pulled HIGH by the VDD signal whenever the ACMP is enabled despite having an internal pull down resistor. This behavior is cause by an internal connection between VDD and GPIO4. Similar behavior can be reproduced when one ACMP's IN+ port is connected to another ACMP's IN+ port.

CH1 (Yellow): ACMP PWR UP (GPI0)
CH3 (Light Blue): Digital IO w/ Analog Input Mode Configuration (GPIO4)
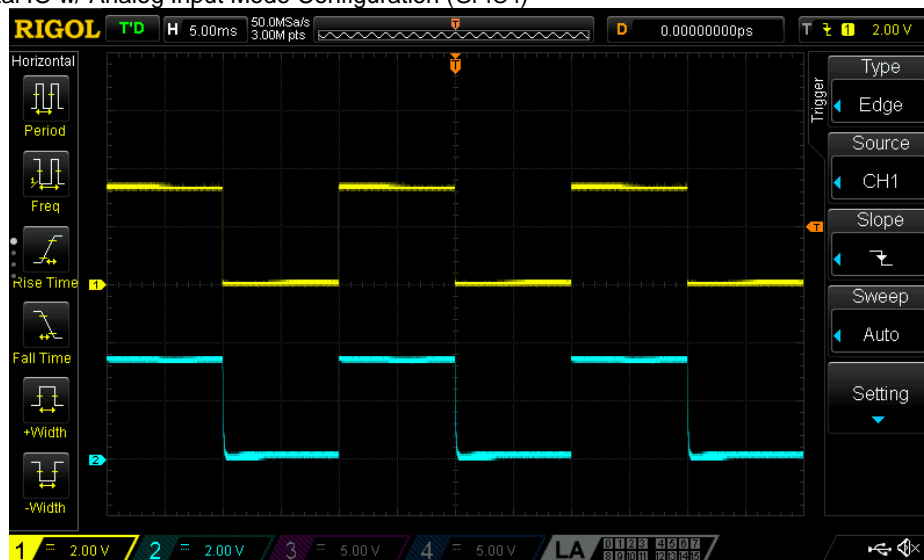
ACMP Input Structure Behavior

Workaround:

If an ACMP is disabled, the GPIO associated with that ACMP will operate as expected under any configuration. Please reference Table 1 above for more information regarding which GPIOs are associated with which ACMPs.

When the ACMPs are enabled, it is possible to inadvertently connect multiple ACMP sources together through the input structure. This is possible when the ACMP input is connected to a source other than its analog GPIO and that GPIO's input mode is set to "Analog IO".

There is no workaround for this behavior. With this in mind, the GPIOs should not be used as digital IOs (with "Input mode" set to Analog input) or as digital outputs (with "Output mode" set to 1/2/4x 3-State Output) if the respective ACMP is enabled and connected to another input source.

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