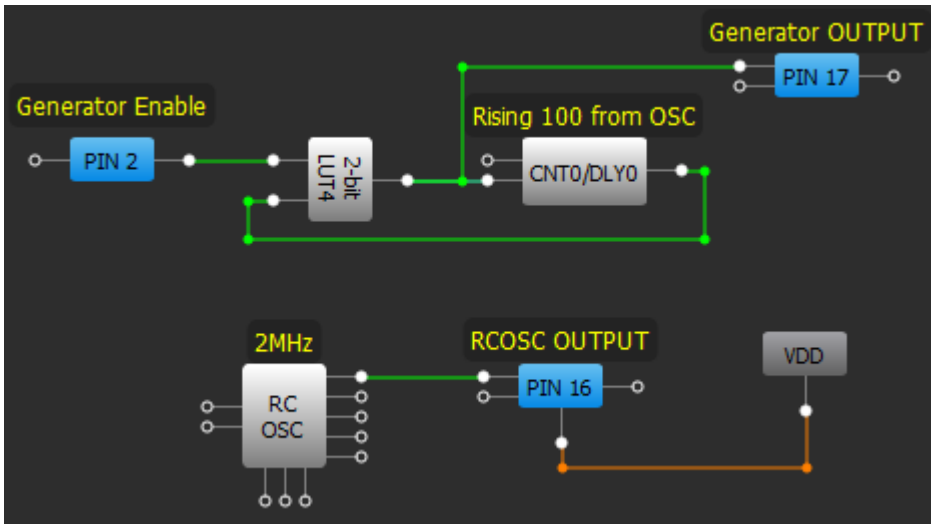
SLG46722

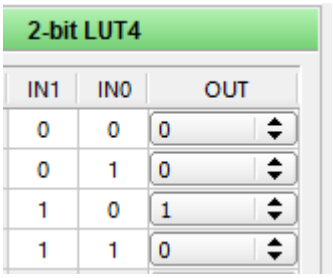
ISSUE 1: Long RC OSC Settling Time
Functional Block Affected: RC OSC, Counter, Delay

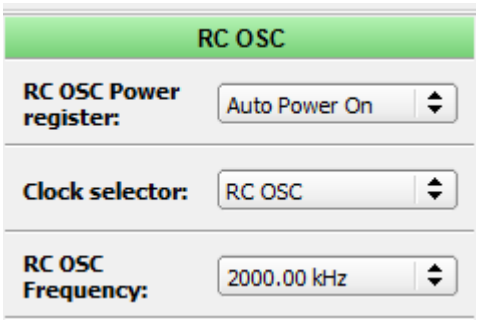
Description:

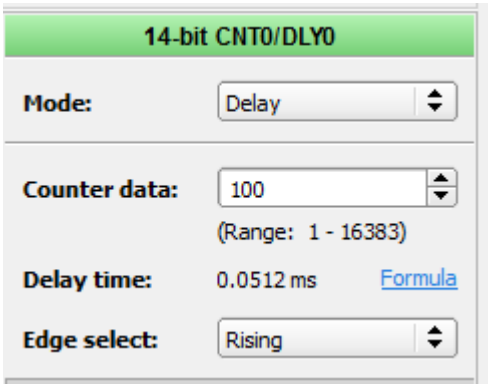
The RC OSC has a longer settling time when configured as 2 MHz with Auto Power On in the designs that have very short RC OSC disable time.

An example of such issue is in the following configuration:

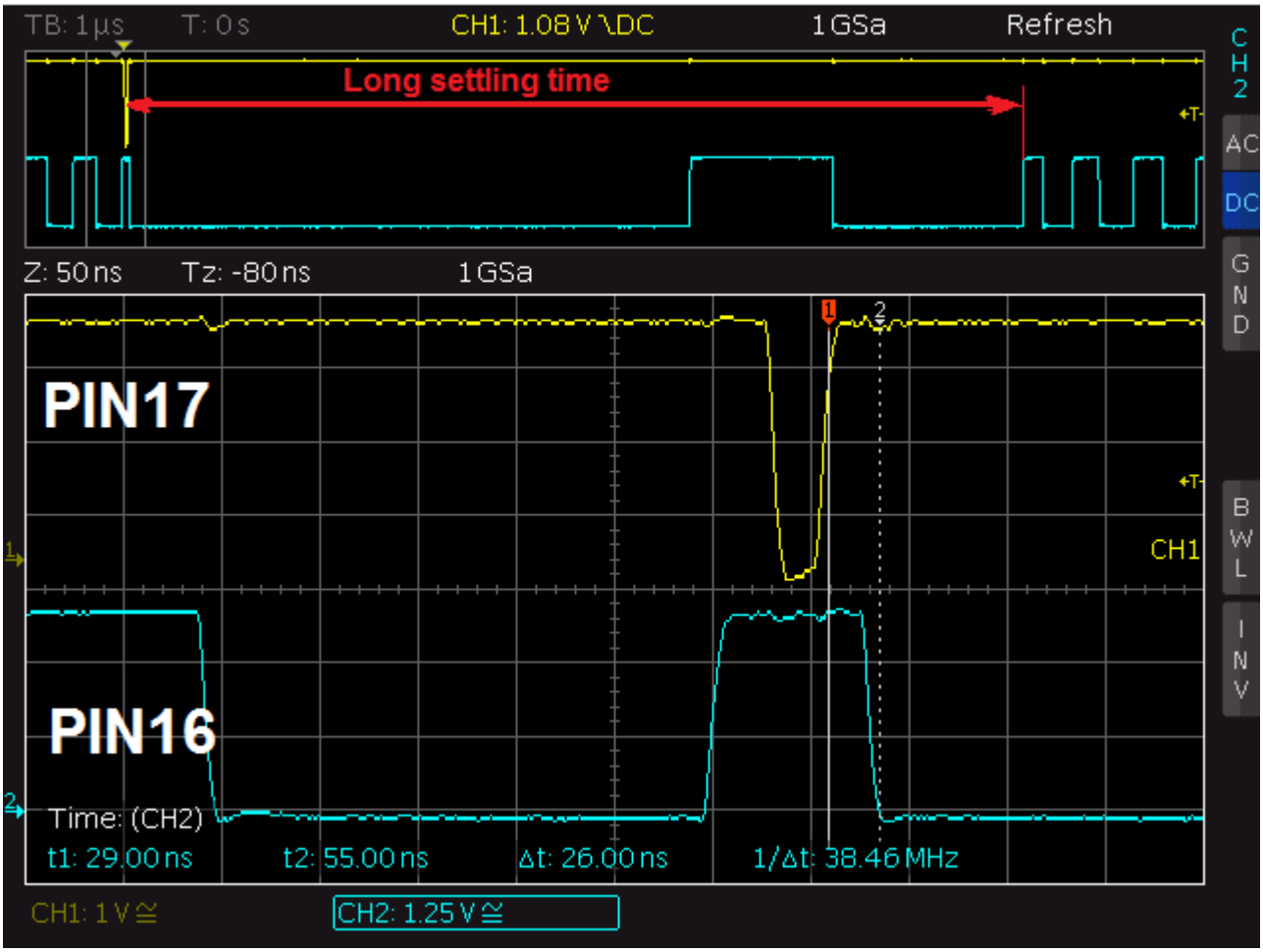








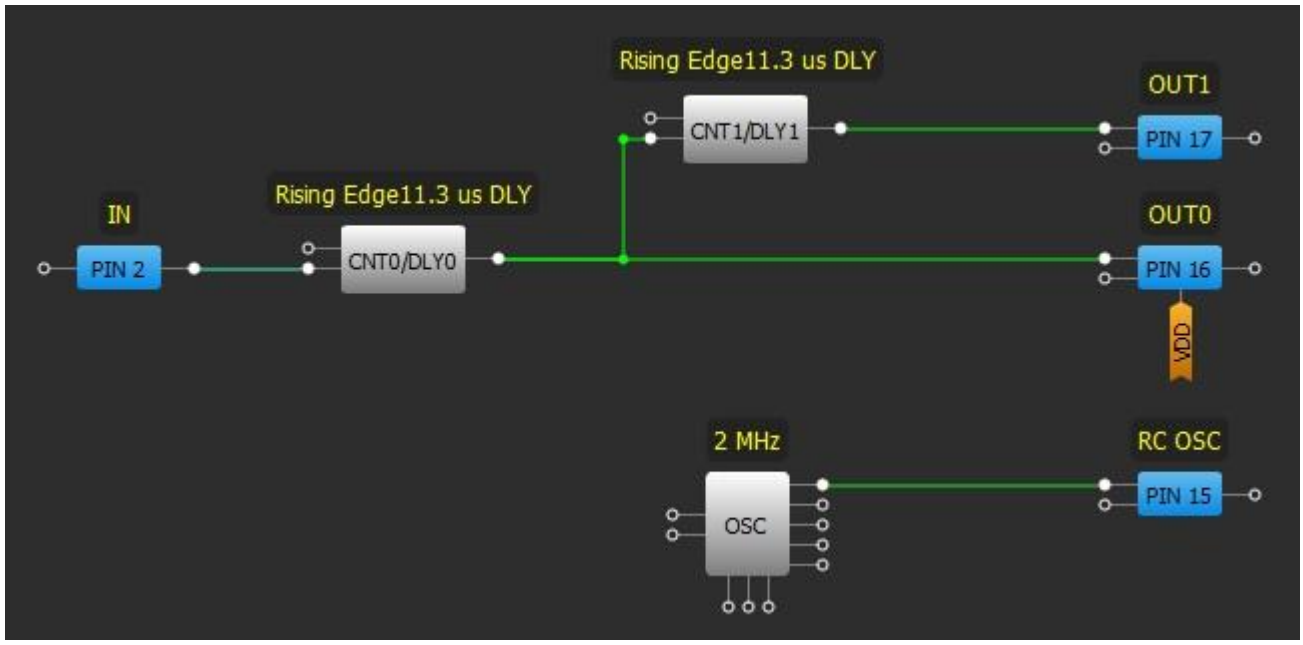
The configuration shown above generates a periodical signal with a frequency defined by the Delay cell and started by a high signal on PIN2. The issue becomes apparent in a longer settling time when the scheme generates short pulses (Delay is configured as a rising edge delay only). See waveform below.

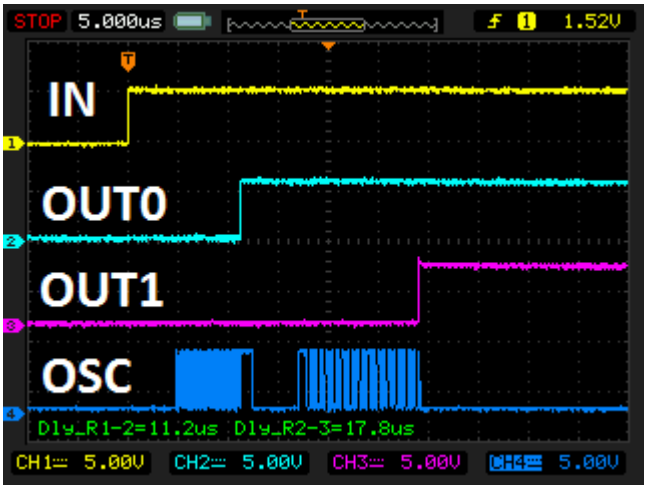


Channel 1 – 2-bit LUT4 output; Channel 2 – RC OSC output

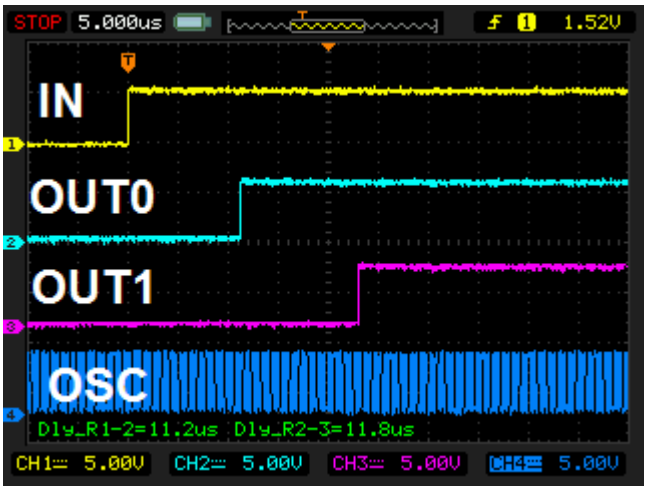
Such behavior will lead to substantial error in period calculations if the delay time is relatively small.

The same situation occurs while using two connected delays (all edge detect types except for a pair “Rising edge DLY – Falling edge DLY”).
In the following example, Delay0 and Delay1 are configured in the same way. However, Delay1 time is 17.8us instead of expected 11.3us (Delay0 time).



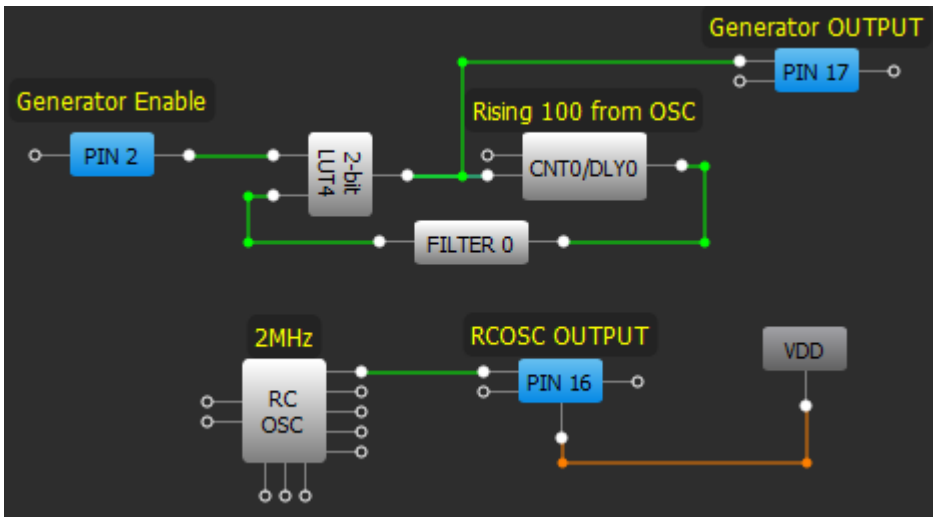


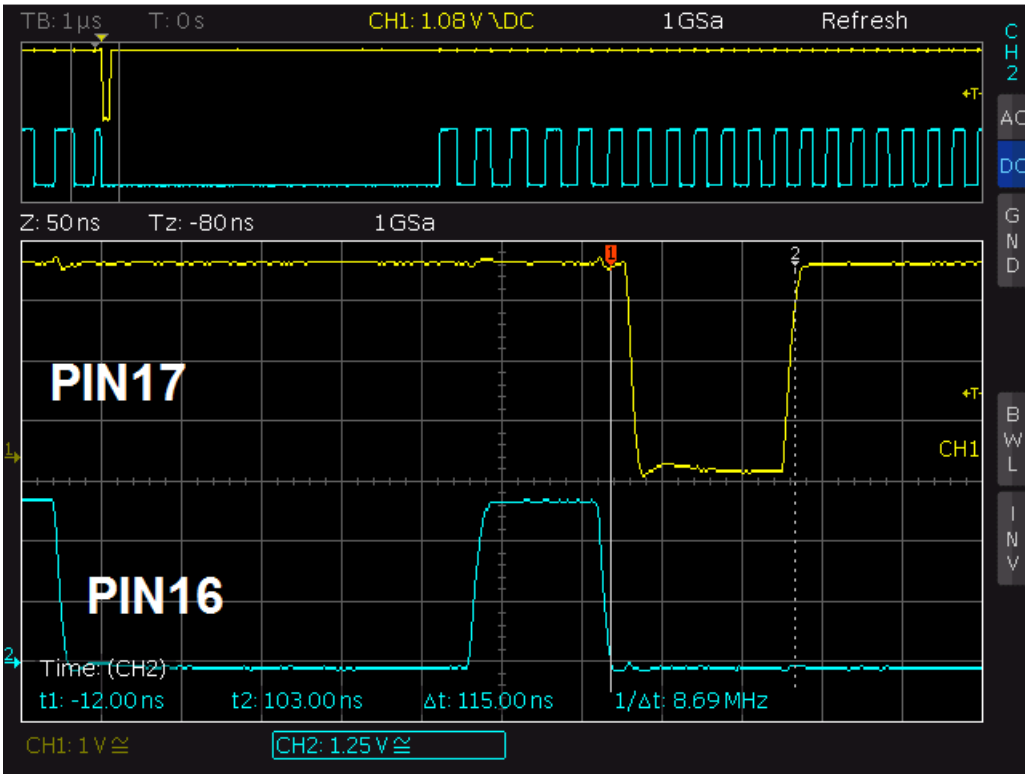
If there are some inner blocks which use RC OSC at the moment or RC OSC is forced power on when such error appears, RC OSC will be operational and delay value will be proper.



Workaround:

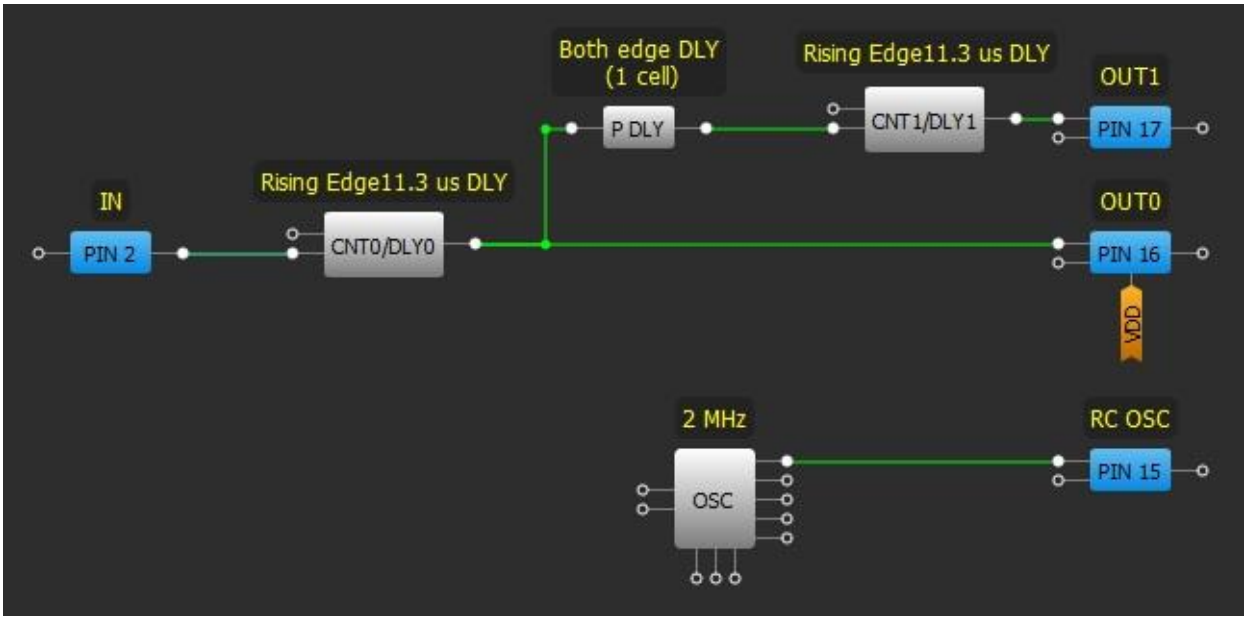
- In first case use block with longer propagation time. For example a Filter cell with an inverted output. Using two Filters in series or P DLY blocks in both edge delay mode (Delay time is 1 cell) for low power supply value (<3.3V) will result in a longer disable RC OSC time.





Channel 1 – 2-bit LUT4 output; Channel 2 – RC OSC output

- Using two delays in series (except for a pair “Rising edge DLY – Falling edge DLY”) use one Filter cell or P DLY between delay blocks. Using LUTs won`t help in this case.

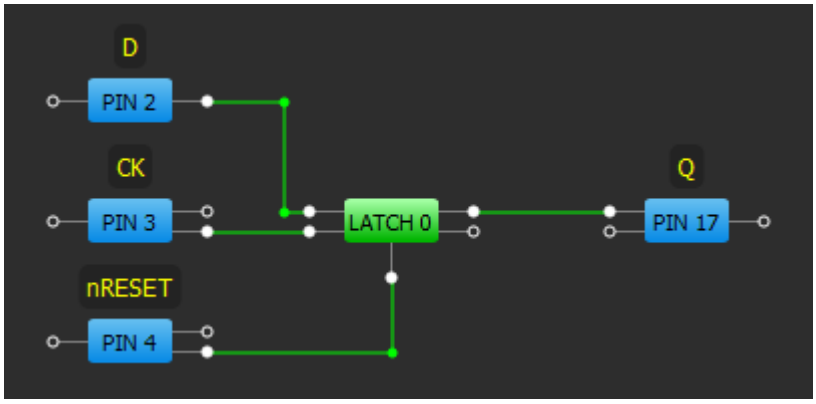


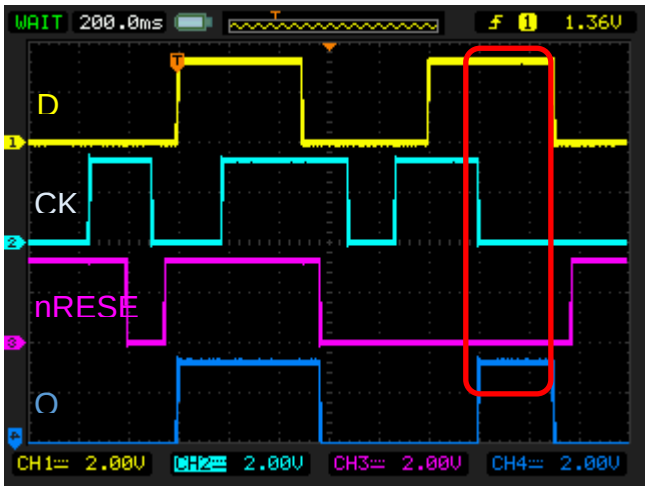
- Use the “Force power on” RC OSC power control option to make the RC OSC operate at all times.

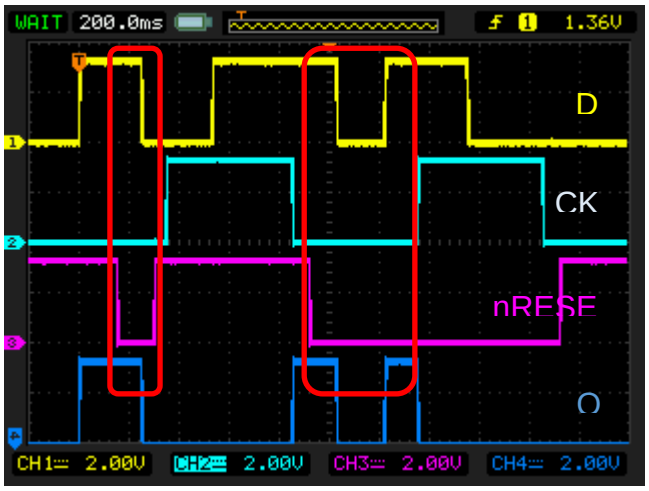
ISSUE 2: LATCH Block nRESET Incorrect Operation
Functional Block Affected: LATCH

Description:

The reset function in LATCH blocks does not operate correctly. This can be described as function failure when nRESET input is set LOW.



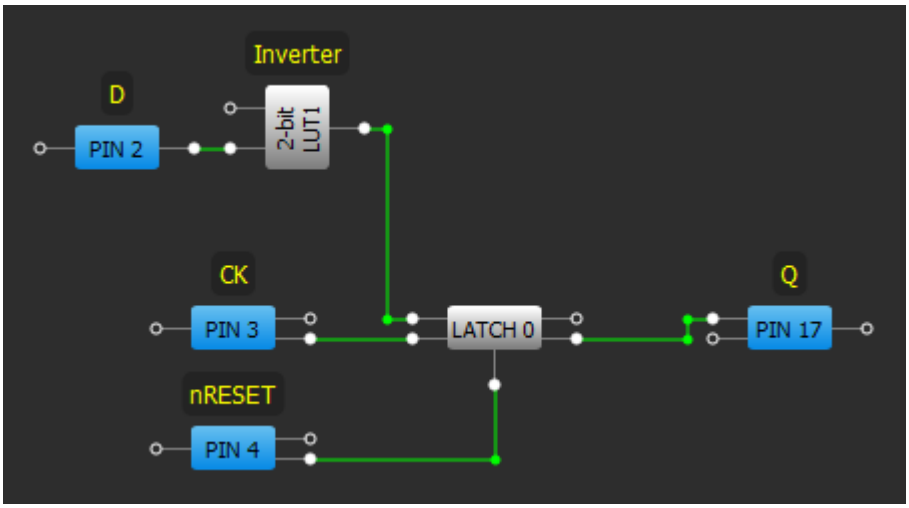


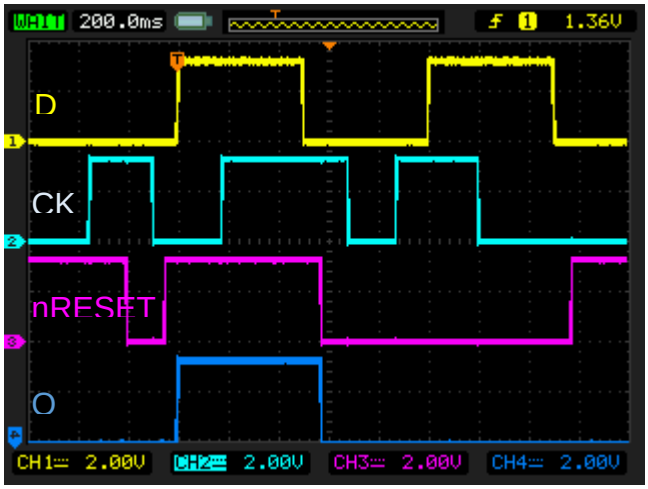


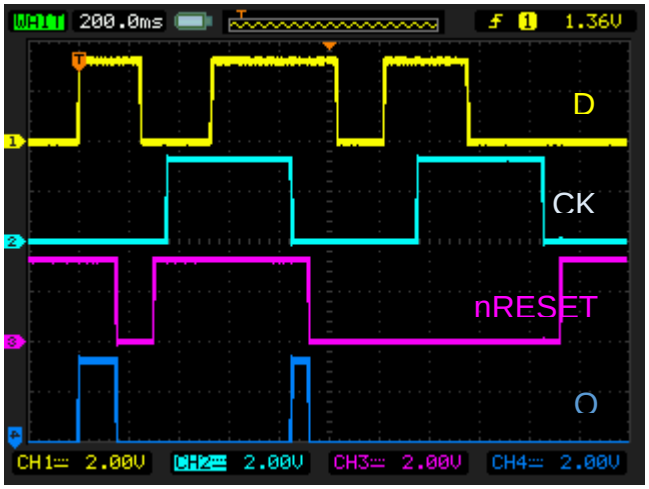
The scope shots shown above show the incorrect nRESET function operation marked with red rectangles. From these waveforms can be seen that the reset function operates only when the CK signal is HIGH, in all other cases it is inoperational.

Workaround:

- Avoid using nRESET function in LATCH blocks in SLG46721/722 devices, if possible use SLG46110/120 devices, where this function operates correctly.
- Use nSET configuration, initial state HIGH, add inverter on D input and use nQ (inverted) output of the LATCH block:





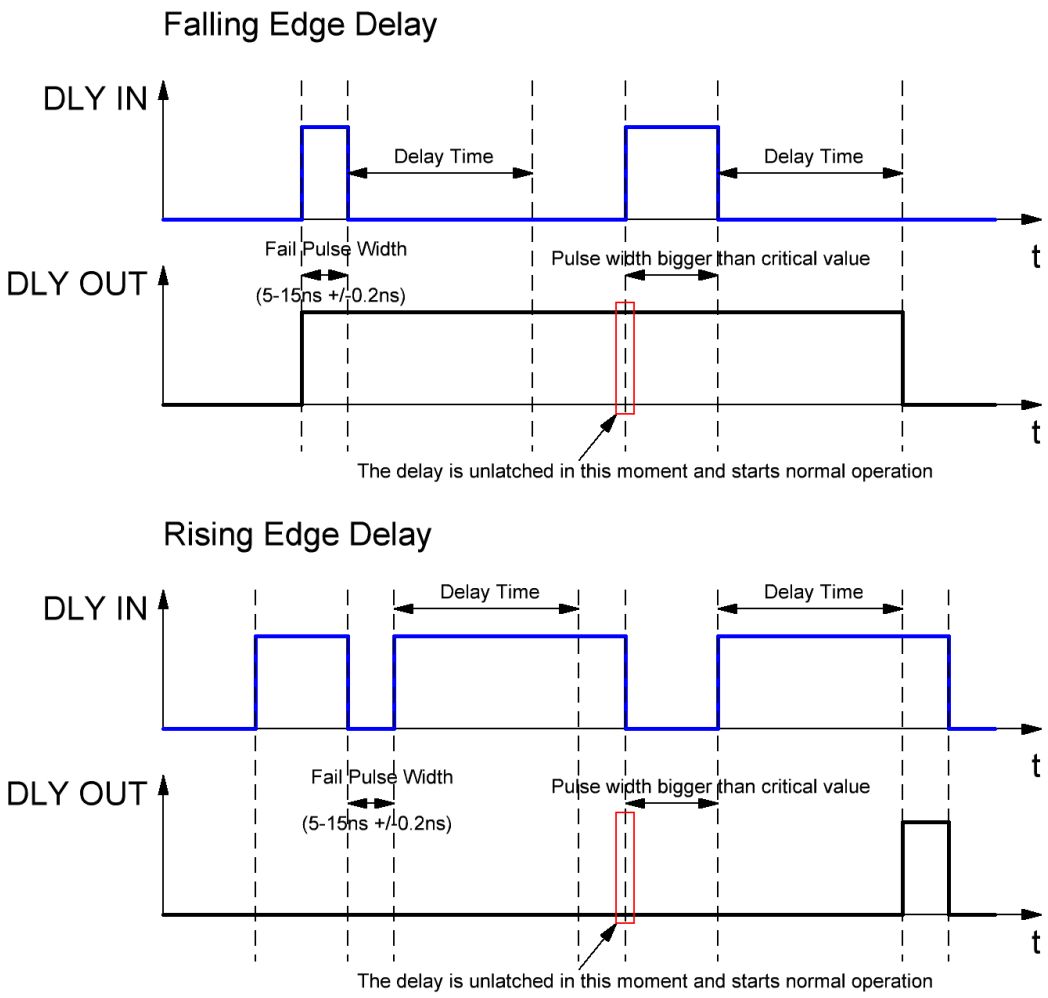


ISSUE 3: Delay Lock-up by a Short Pulse
Functional Block Affected: Delay

Description:

The delay output could be latched despite the input change when a short pulse is input. For example, if the delay cell is configured as a falling edge delay, the short pulse (see NOTE) appears on its input the delay cell output will switch from LOW to HIGH but may not switch from HIGH to LOW even after the delay time has passed.

NOTE: The pulse width varies from chip to chip and with different VDD voltage. It is in range of 5-15ns and in the window +/-0.2ns, so it should be very precise for issue happen.



Also, note that both edge delays do not have such issue.

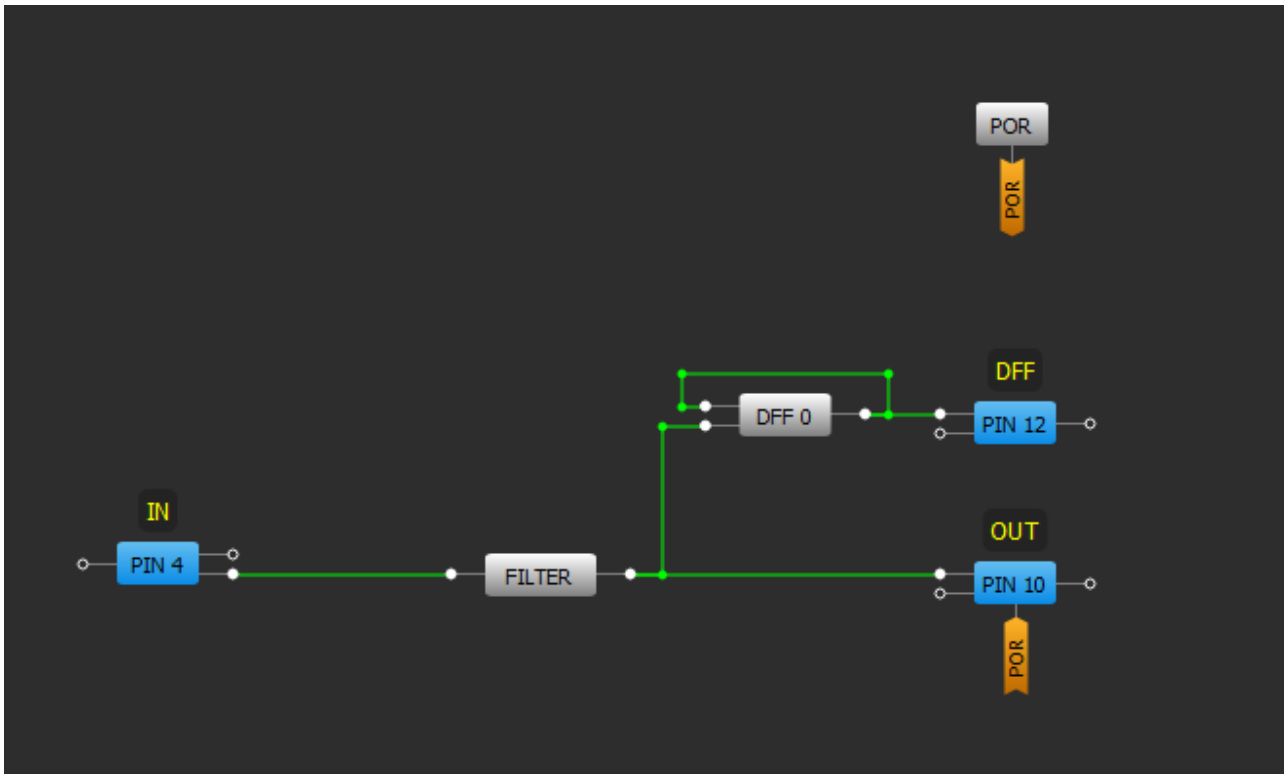
Workaround:

- Use FILTER block on the Delay block input;
- Use P DLY block configured as a both edge delay.

ISSUE 4: FILTER cell does not filter out glitches
Functional Block Affected: FILTER

Description:

If clock type high frequency input comes in, the FILTER cell may not filter out it. There are several factors like input frequency, duty cycle and LOW duration in such signal that may lead to its passing through FILTER block.



Channel 1 (yellow/top line) – PIN#4 (IN)
Channel 2 (light blue/2nd line) – PIN#10 (OUT)
Channel 3 (magenta /3rd line) – PIN#12 (DFF)

1. Period is 60ns. Pulse width is 10ns DC=16.7% (Correct functionality)

2. Period is 60ns. Pulse width is 20ns DC = 33.3% (Incorrect functionality)

3. Period is 60ns. Pulse width is 30ns DC=50% (Incorrect functionality)

4. Period is 60ns. Pulse width is 40ns DC=66.67% (Correct functionality)

Workaround:

Currently there is no workaround for this issue. Filter block is good at filtering short spontaneous glitches. It is intended to be used in series connection before the delay cell to avoid its latching (see issue #4).

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