## SLG46120

ISSUE 1: Long RC OSC Settling Time
Functional Block Affected: RC OSC, Counter, Delay

Description:

The RC OSC has a longer settling time when configured as 2 MHz with Auto Power On in the designs that have very short RC OSC disable time.

An example of such issue is in the following configuration:

The configuration shown above generates a periodical signal with a frequency defined by the Delay cell and started by a HIGH signal on PIN2. The issue becomes apparent in a longer settling time when the scheme generates short pulses (Delay is configured as a rising edge delay only). See waveform below.
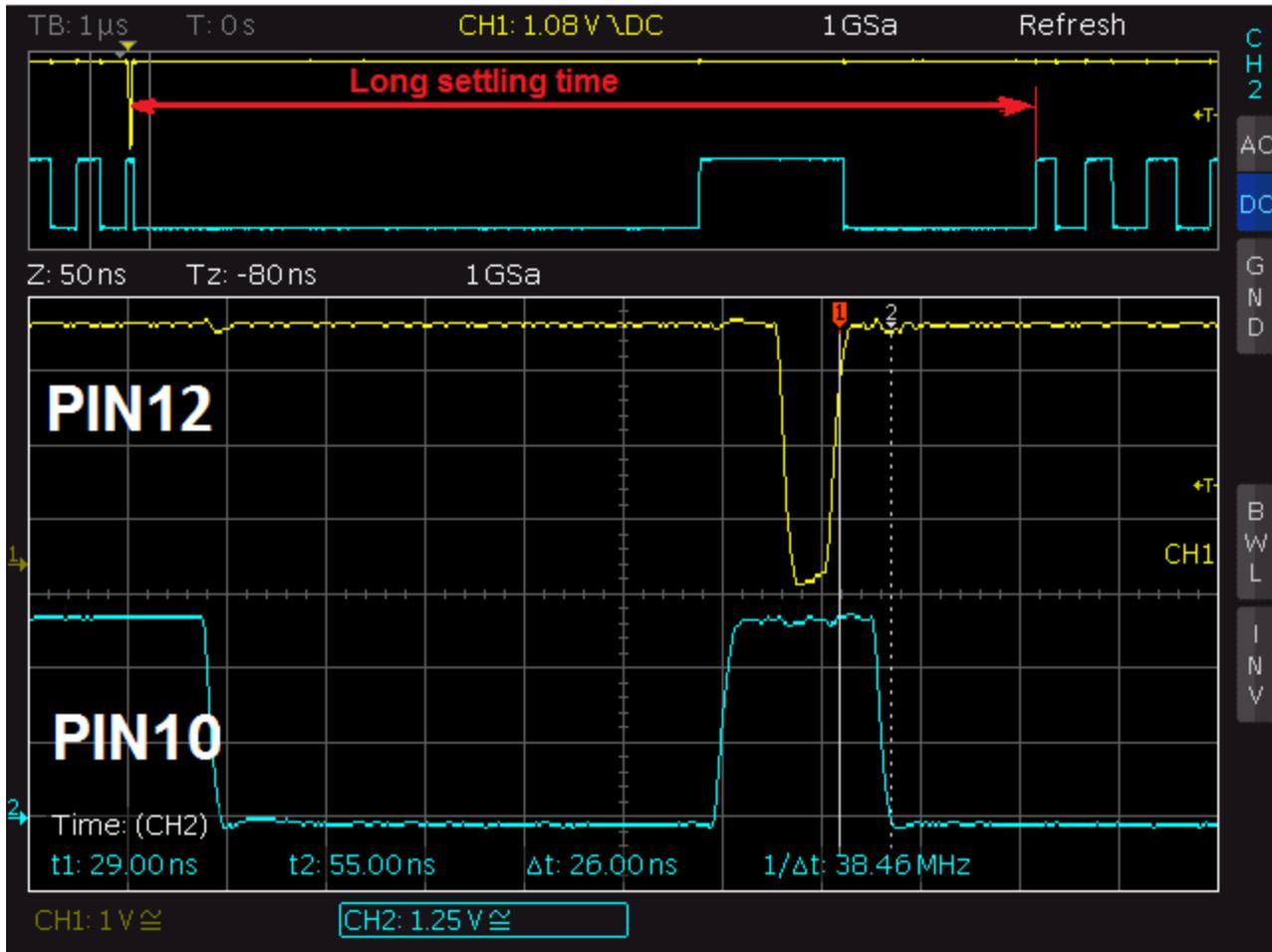
Channel 1 – 2-bit LUT0 output; Channel 2 – RC OSC output

Such behavior will lead to substantial error in period calculations if the delay time is relatively small.

The same situation occurs while using two connected delays (all edge detect types except for a pair "Rising edge DLY – Falling edge DLY").

In the following example, Delay0 and Delay1 are configured in the same way. However, Delay1 time is 17.8us instead of expected 11.3us (Delay0 time).
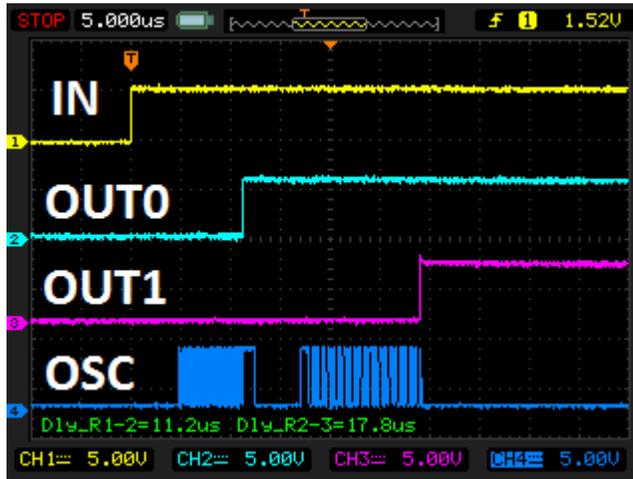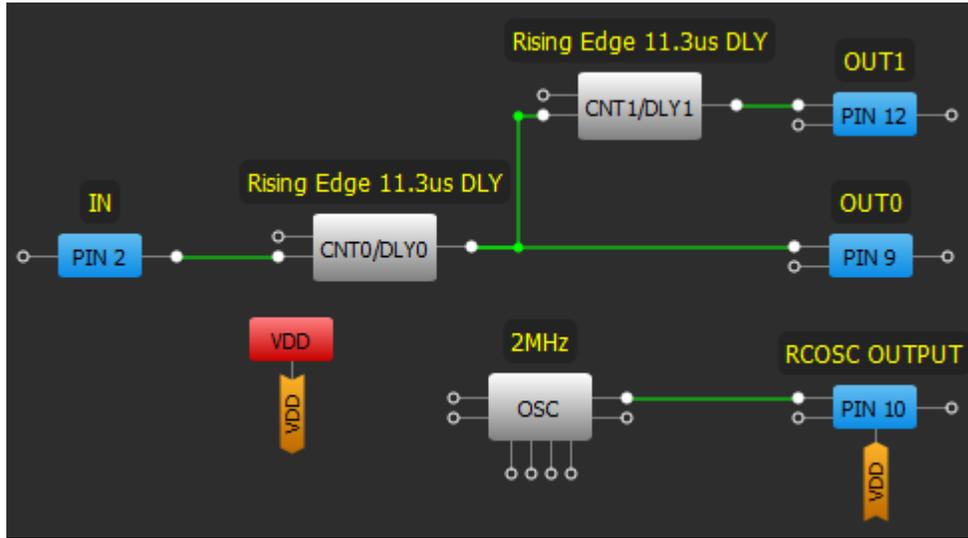
If there are some inner blocks which use RC OSC at the moment or RC OSC is forced power on when such error appears, RC OSC will be operational and delay value will be proper.
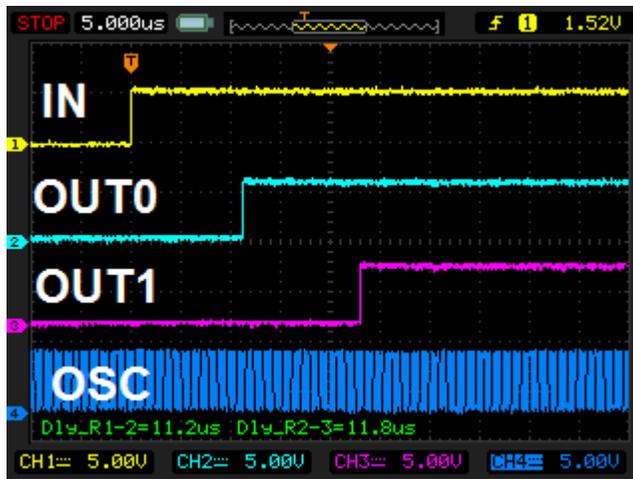
Workaround:

- In first case use block with longer propagation time.
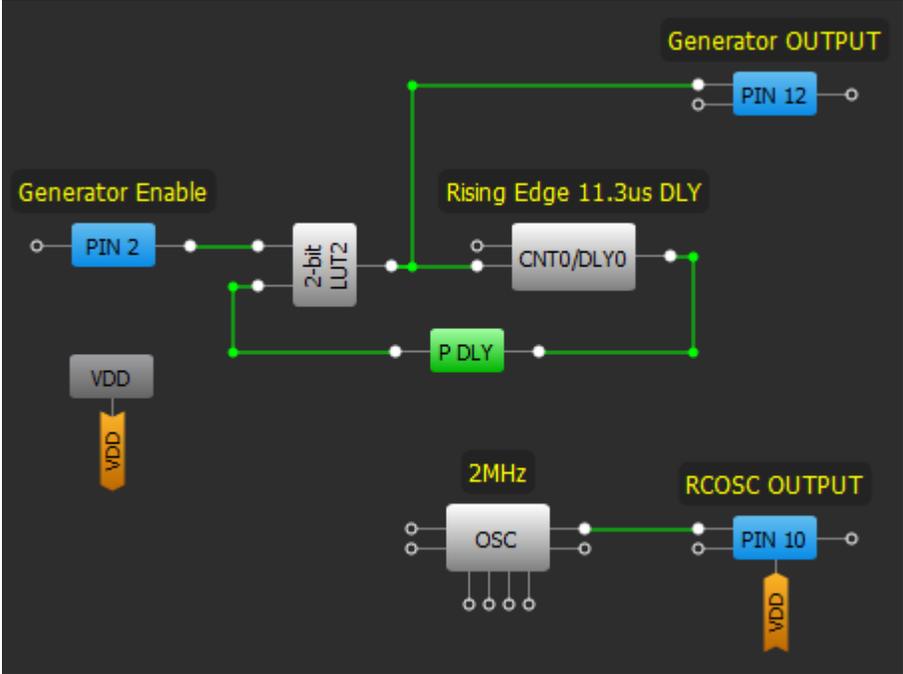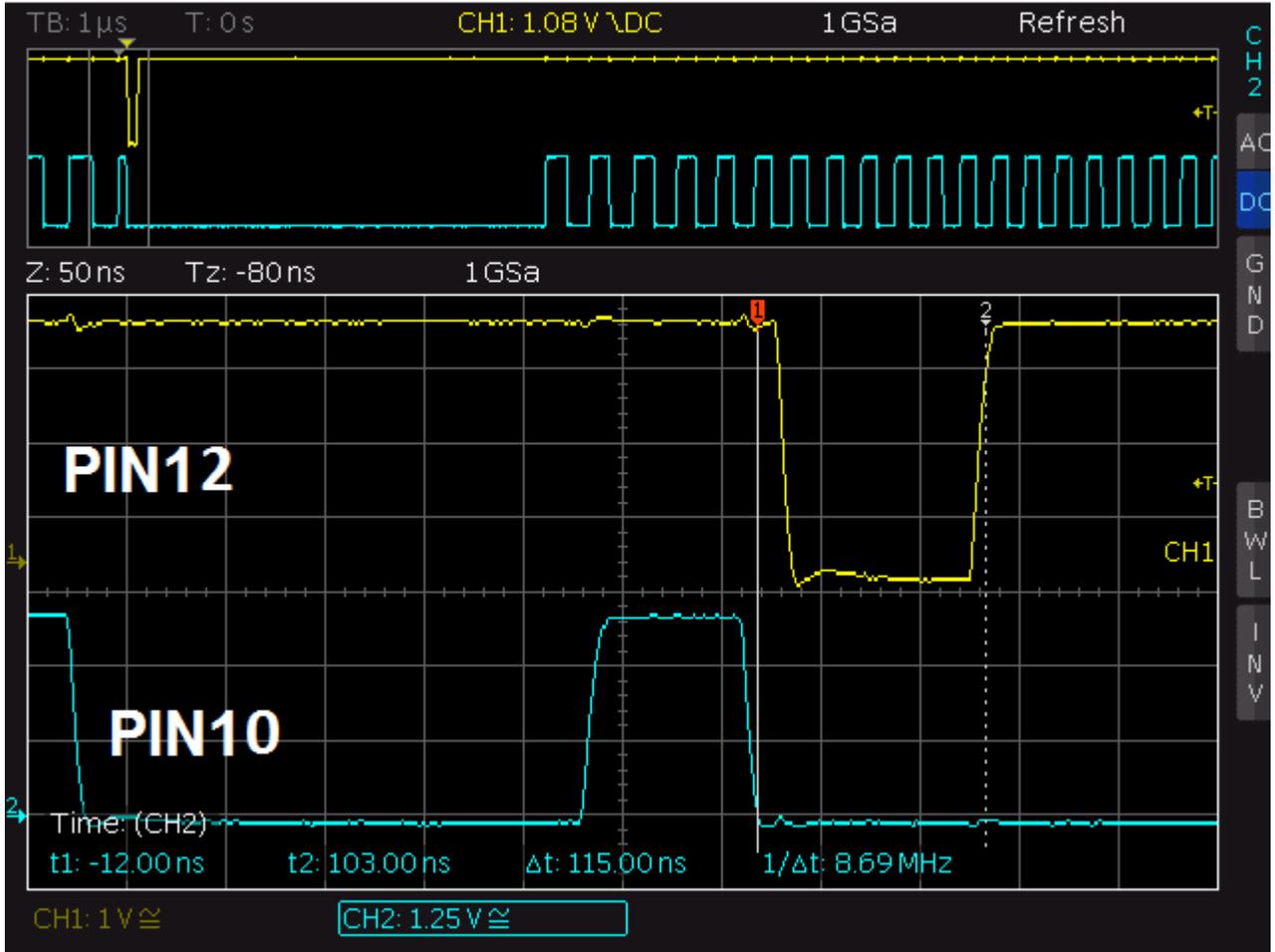
Channel 1 – 2-bit LUT0 output; Channel 2 – RC OSC output

Using two delays in series (except for a pair "Rising edge DLY – Falling edge DLY") use one Filter cell or P DLY between delay blocks. Using LUTs won`t help in this case.
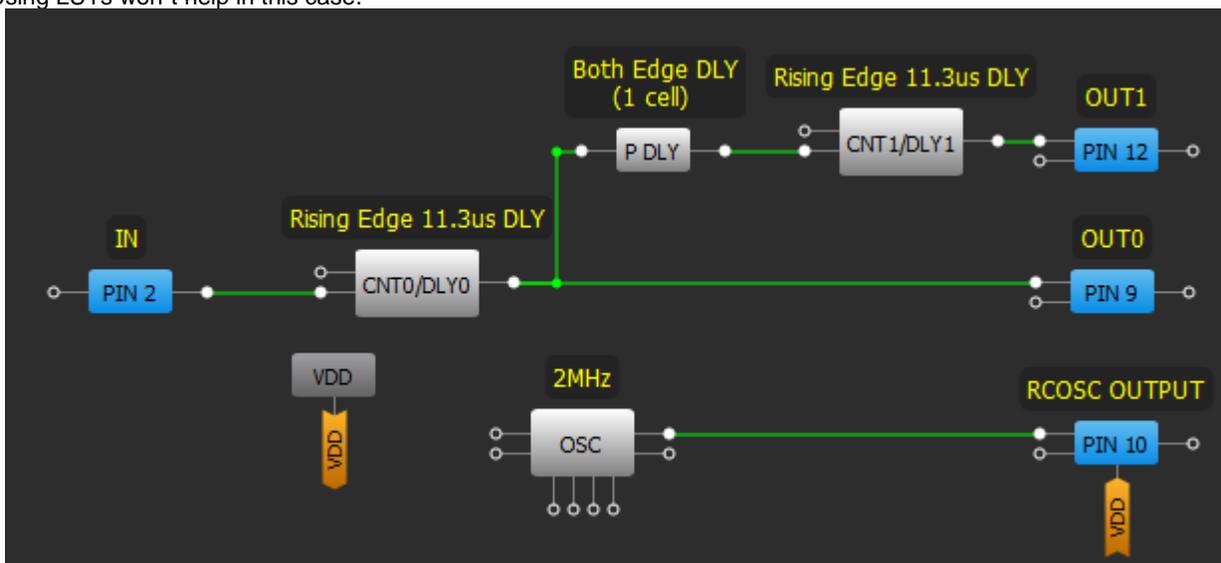
- ▪ Use the "Force power on" RC OSC power control option to make the RC OSC operate at all times.

_____

ISSUE 2: Glitches on ACMP output
## Functional Block Affected: ACMP
Description:

In some cases, ACMP may have short high-level glitches on its output (even if IN+ voltage is less than IN- voltage) after GreenPAK chip being powered up. Such cases may appear when using ACMP with Low Bandwidth mode enabled and Power Up is connected directly to the VDD.

Conditions of glitches appearing are determined by IN- voltage, VDD value and VDD Ramp (see example tables below).

IN- Voltage, mV	VDD, V	VDD Ramp Time	Glitch presence
50	1.8	10 us	+
50	1.8	1 s	-
50	3.3	10 us	+
50	3.3	1 s	+
50	5.5	10 us	+
50	5.5	1 s	+
600	1.8	10 us	-
600	1.8	1 s	-
600	3.3	10 us	+
600	3.3	1 s	+
600	5.5	10 us	+
600	5.5	1 s	+
1200	1.8	10 us	-
1200	1.8	1 s	-
1200	3.3	10 us	-
1200	3.3	1 s	-
1200	5.5	10 us	+
1200	5.5	1 s	-

In order to detect such glitches, scheme with additional LUT was used. This LUT detects high level on ACMP output and stays high until chip powers down.
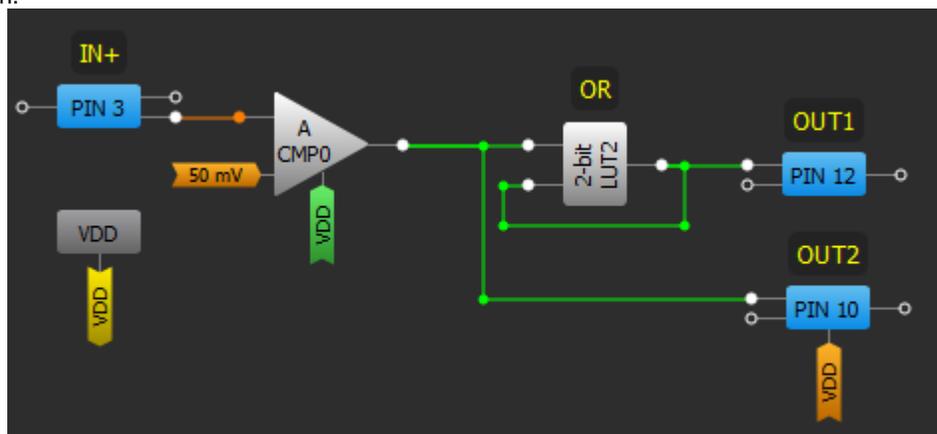
ACMP IN+ is connected to the Ground.
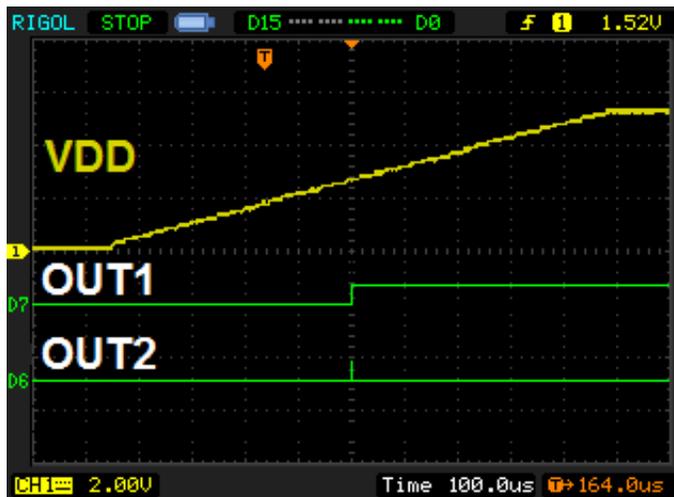
Workaround:

- Use POR block, connected to the ACMP`s Power Up pin. However, in this case ACMP will start working with low level output and will be able to go high only after POR goes high + ACMP power on time.

_____
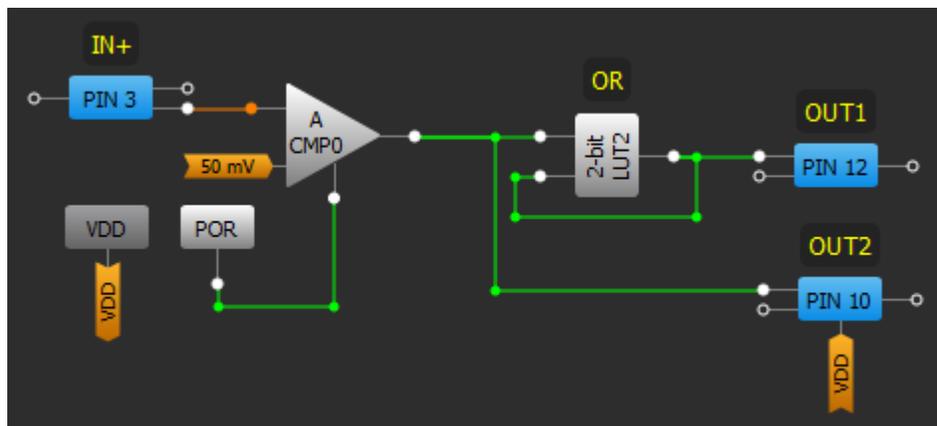
ISSUE 3: Delay Lock-up by a Short Pulse
Functional Block Affected: Delay

Description:

The delay output could be latched despite the input change when a short pulse is input. For example, if the delay cell is configured as a falling edge delay, the short pulse (see NOTEs) appears on its input the delay cell output will switch from LOW to HIGH but may not switch from HIGH to LOW even after the delay time has passed.

NOTE1: The pulse width that causes the fail varies from chip to chip and with different VDD voltage. It is in range of 5-15ns and in the window +/-0.2ns, so it should be very precise for issue to happen.

NOTE 2: The issue happens even with OSC being forced power on. The following timing diagrams show OSC in auto power on mode.

![dialog SEMICONDUCTOR]

SLG46120

Rising edge delay, normal operation
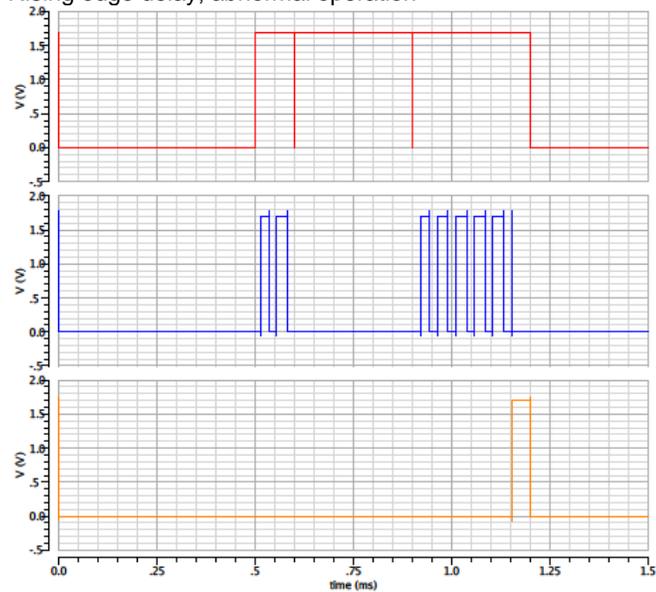
Delay input
first glitch width >15ns
second glitch width >15ns

OSC Output

Delay output

Rising edge delay, abnormal operation

Delay input
first glitch width 5-15ns +/-0.2ns
second glitch width >15ns

OSC Output

Delay output

Rising edge delay, abnormal operation

Delay input
first glitch width 5-15ns +/-0.2ns
second glitch width >15ns

OSC Output

Delay output

Falling edge delay, normal operation

Delay input
first glitch width >15ns
second glitch width >15ns

OSC Output

Delay output

Falling edge delay, abnormal operation
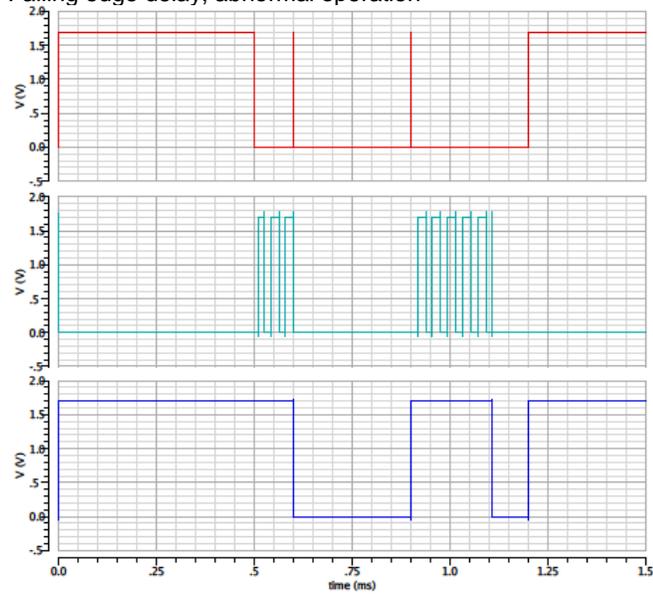
Delay input
first glitch width 5-15ns +/-0.2ns
second glitch width >15ns

OSC Output

Delay output

Falling edge delay, abnormal operation

Delay input
first glitch width 5-15ns +/-0.2ns
second glitch width >15ns

OSC Output

Delay output

Both edge delay, normal operation
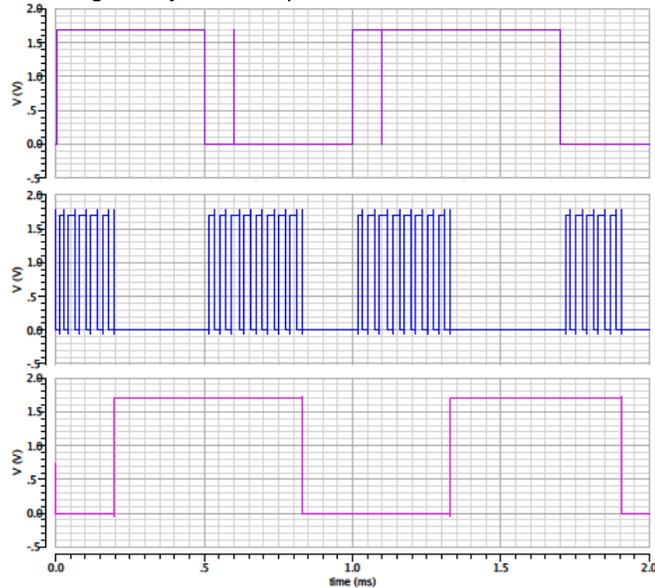
Delay input
first glitch width >15ns
second glitch width >15ns

OSC Output

Delay output

Both edge delay, abnormal operation
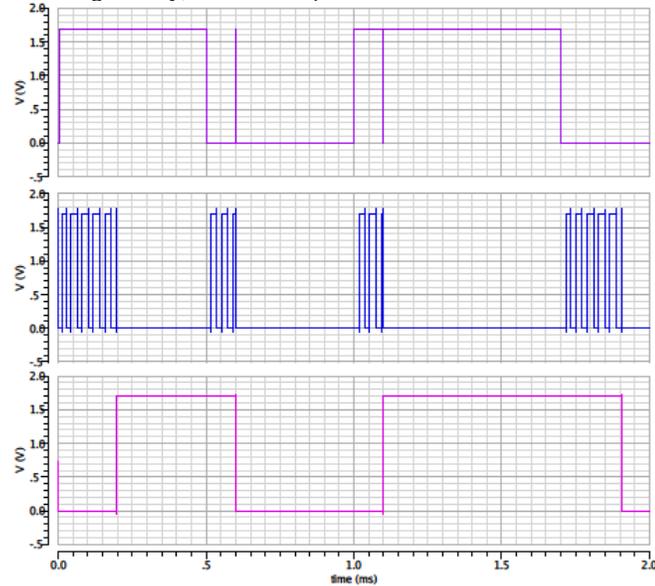
Delay input
first glitch width 5-15ns +/-0.2ns
second glitch width >15ns

OSC Output

Delay output

Workaround:

- Use P DLY/FILTER block configured as a both edge delay or a FILTER.
- Use a combination of external RC filter an input PIN configured a Digital input with Schmitt trigger if a glitchy signal comes from external source.

ISSUE 4: Device Damage by High Input Voltage on External Vref PIN of ACMP
Functional Block Affected: ACMPs

Description:

The device may be damaged by the voltage higher than 2V applied to IN- of ACMP as an external reference voltage.

Workaround:

- There is no workaround to this issue, avoid applying more than 2V on IN- of ACMP used as external voltage reference.

_____

ISSUE 5: FILTER cell does not filter out glitches
Functional Block Affected: FILTER

Description:

If clock type high frequency input comes in, the FILTER cell may not filter out it. There are several factors like input frequency, duty cycle and LOW duration in such signal that may lead to its passing through FILTER block.
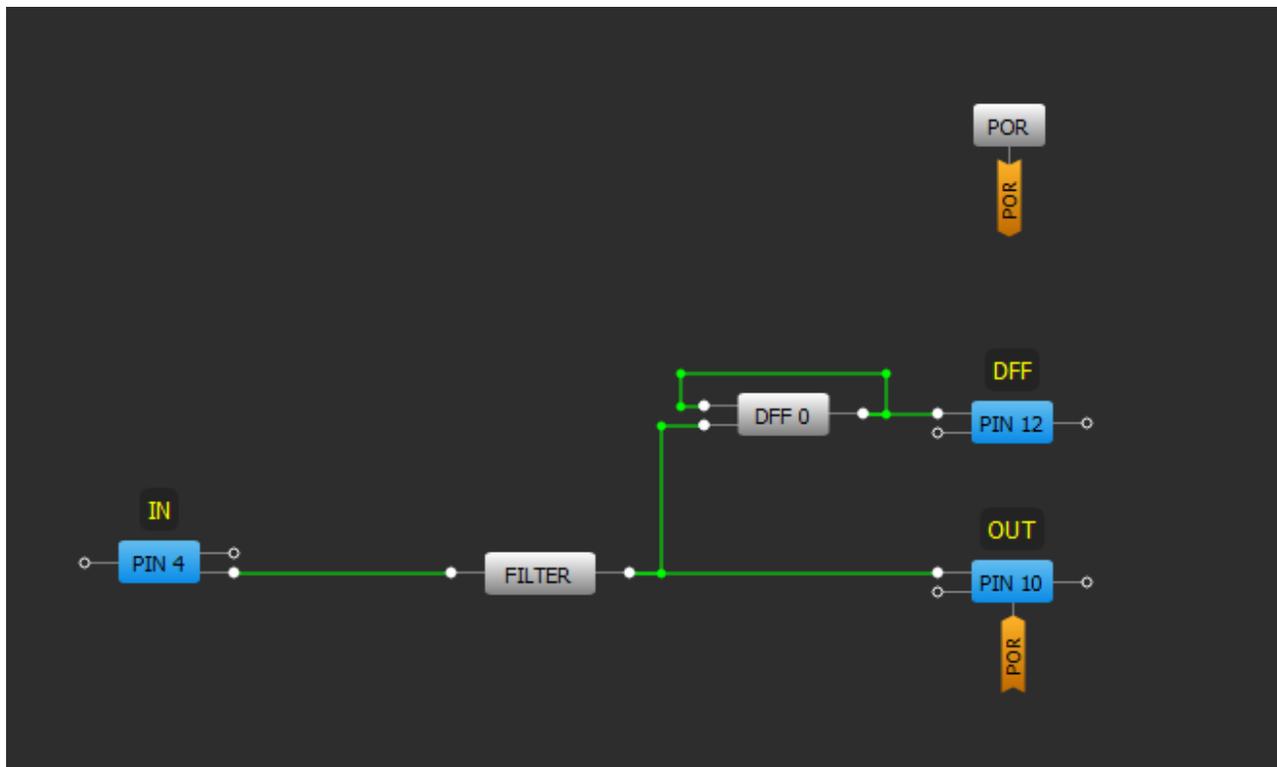
Channel 1 (yellow/top line) – PIN#4 (IN)
Channel 2 (light blue/2nd line) – PIN#10 (OUT)
Channel 3 (magenta /3rd line) – PIN#12 (DFF)

1. Period is 60ns. Pulse width is 10ns DC=16.7% (Correct functionality)

2. Period is 60ns. Pulse width is 20ns DC = 33.3% (Incorrect functionality)

3. Period is 60ns. Pulse width is 30ns DC=50% (Incorrect functionality)

4. Period is 60ns. Pulse width is 40ns DC=66.67% (Correct functionality)
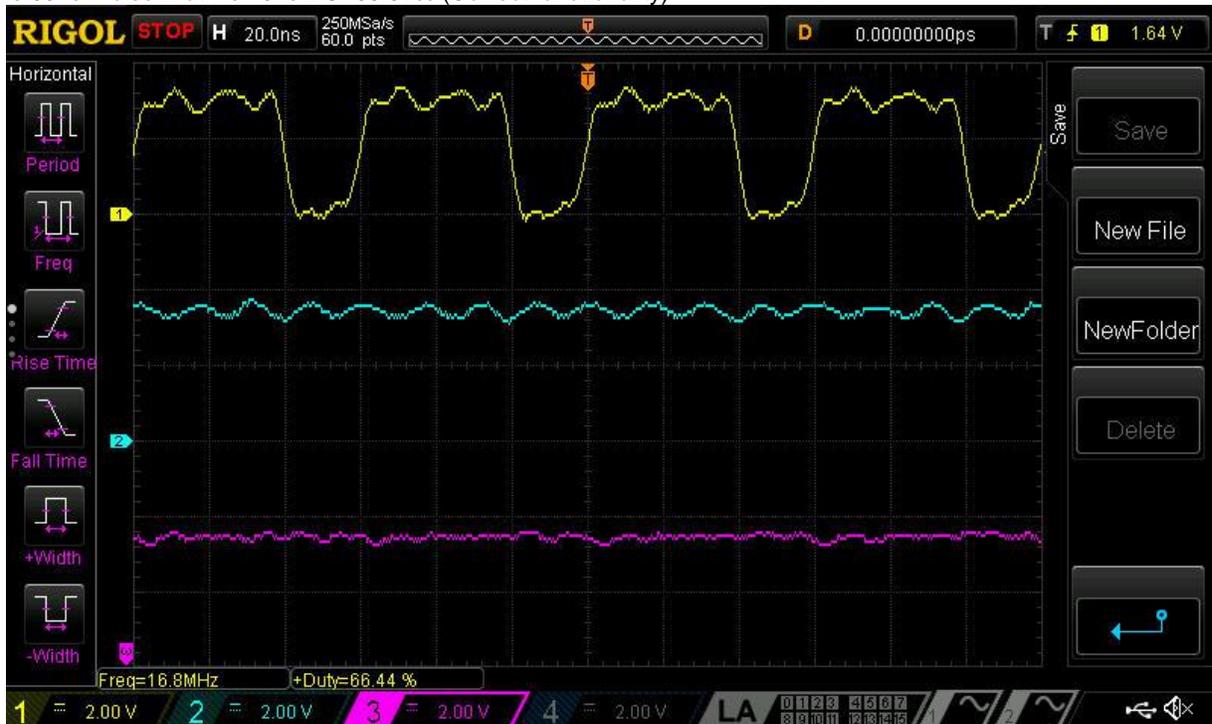
<u>*Workaround:*</u>

Currently there is no workaround for this issue. Filter block is good at filtering short spontaneous glitches. It is intended to be used in series connection before the delay cell to avoid its latching (see issue #5).

Disclaimer

Information in this document is believed to be accurate and reliable. However, Dialog Semiconductor does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information. Dialog Semiconductor furthermore takes no responsibility whatsoever for the content in this document if provided by any information source outside of Dialog Semiconductor.

Dialog Semiconductor reserves the right to change without notice the information published in this document, including without limitation the specification and design of the related semiconductor products, software and applications.

Applications, software, and semiconductor products described in this document are for illustrative purposes only. Dialog Semiconductor makes no representation or warranty that such applications, software and semiconductor products will be suitable for the specified use without further testing or modification. Unless otherwise agreed in writing, such testing or modification is the sole responsibility of the customer and Dialog Semiconductor excludes all liability in this respect.

Customer notes that nothing in this document may be construed as a license for customer to use the Dialog Semi-conductor products, software and applications referred to in this document. Such license must be separately sought by customer with Dialog Semiconductor.

All use of Dialog Semiconductor products, software and applications referred to in this document are subject to Dialog Semiconductor's Standard Terms and Conditions of Sale, available on the company website (www.dialog-semiconductor.com) unless otherwise stated.

Dialog and the Dialog logo are trademarks of Dialog Semiconductor plc or its subsidiaries. All other product or service names are the property of their respective owners.

RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

Contacting Dialog Semiconductor

United Kingdom (Headquarters)
Dialog Semiconductor (UK) LTD
Phone: +44 1793 757700

Germany
Dialog Semiconductor GmbH
Phone: +49 7021 805-0

The Netherlands
Dialog Semiconductor B.V.
Phone: +31 73 640 8822

Email:
enquiry@diasemi.com

North America
Dialog Semiconductor Inc.
Phone: +1 408 845 8500

Japan
Dialog Semiconductor K. K.
Phone: +81 3 5769 5100

Taiwan
Dialog Semiconductor Taiwan
Phone: +886 281 786 222

Web site:
www.dialog-semiconductor.com

Hong Kong
Dialog Semiconductor Hong Kong
Phone: +852 2607 4271

Korea
Dialog Semiconductor Korea
Phone: +82 2 3469 8200

China (Shenzhen)
Dialog Semiconductor China
Phone: +86 755 2981 3669

China (Shanghai)
Dialog Semiconductor China
Phone: +86 21 5424 9058