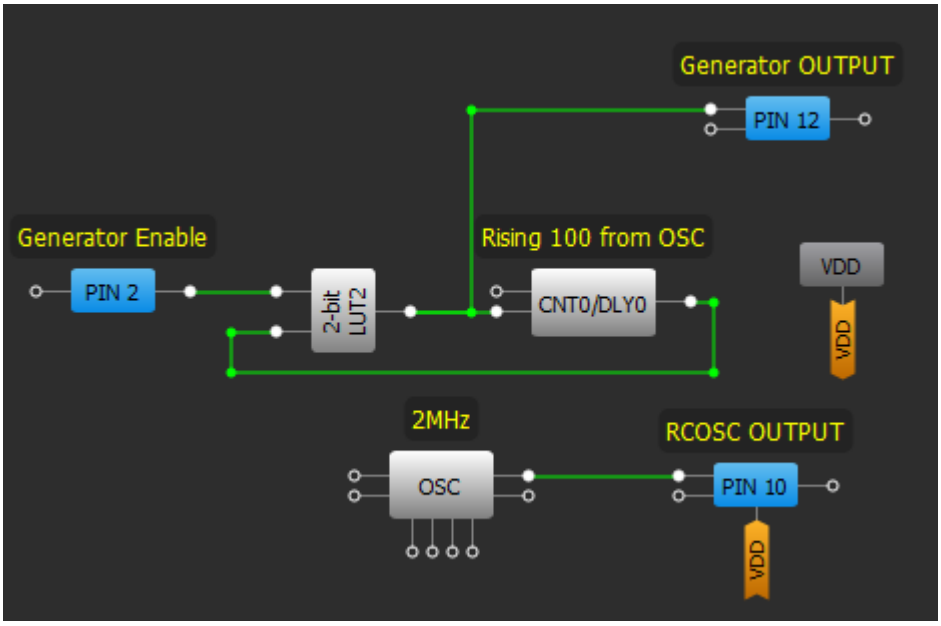
ISSUE 1: Long RC OSC Settling Time
Functional Block Affected: RC OSC, Counter, Delay

Description:

The RC OSC has a longer settling time when configured as 2 MHz with Auto Power On in the designs that have very short RC OSC disable time.

An example of such issue is in the following configuration:



2-bit LUT2

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0

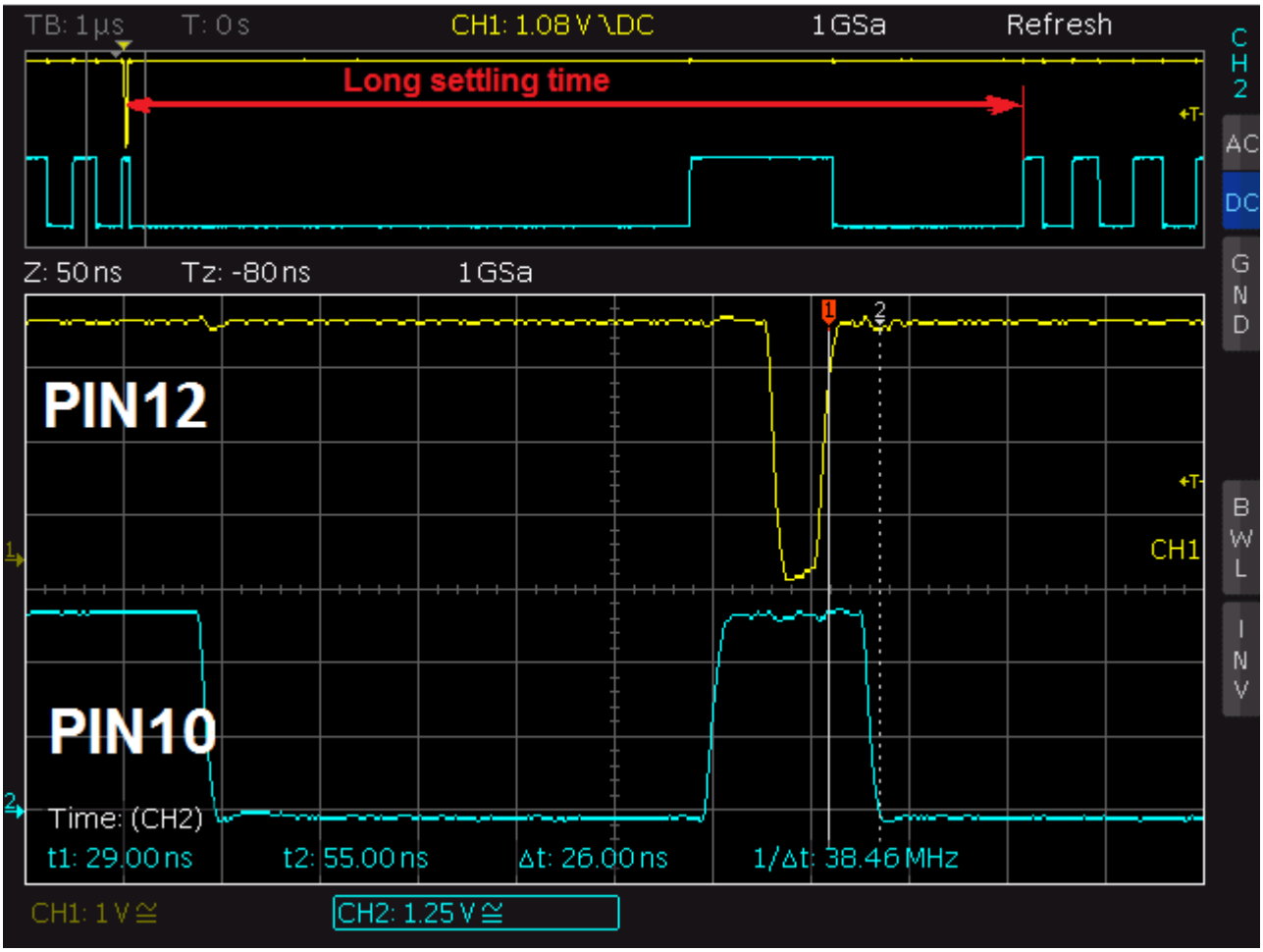
RC OSC

RC OSC Power register:	Auto Power On
Clock selector:	RC OSC
RC OSC Frequency:	2000.00 kHz

14-bit CNT0/DLY0

Mode:	Delay
Counter data:	100
	(Range: 1 - 16383)
Delay time:	0.0512 ms Formula
Edge select:	Rising

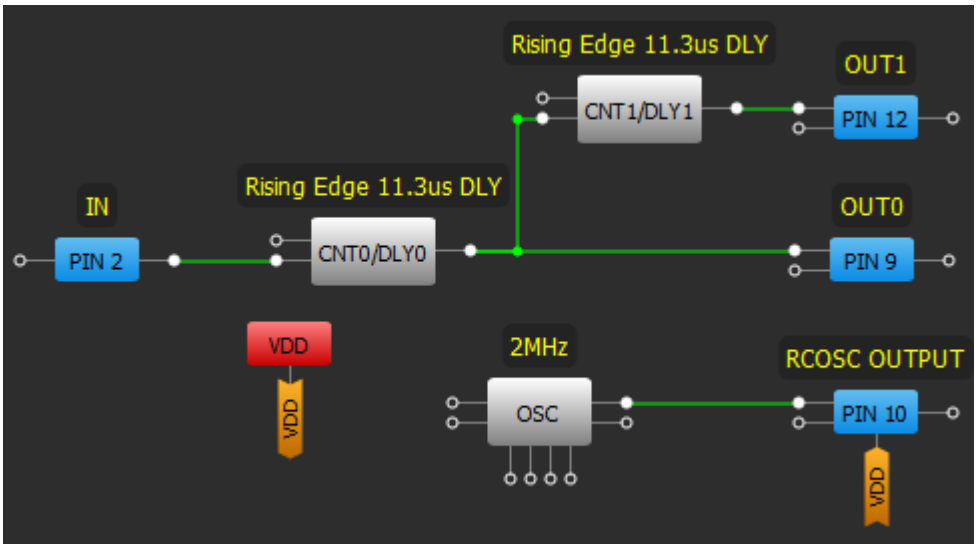
The configuration shown above generates a periodical signal with a frequency defined by the Delay cell and started by a HIGH signal on PIN2. The issue becomes apparent in a longer settling time when the scheme generates short pulses (Delay is configured as a rising edge delay only). See waveform below.

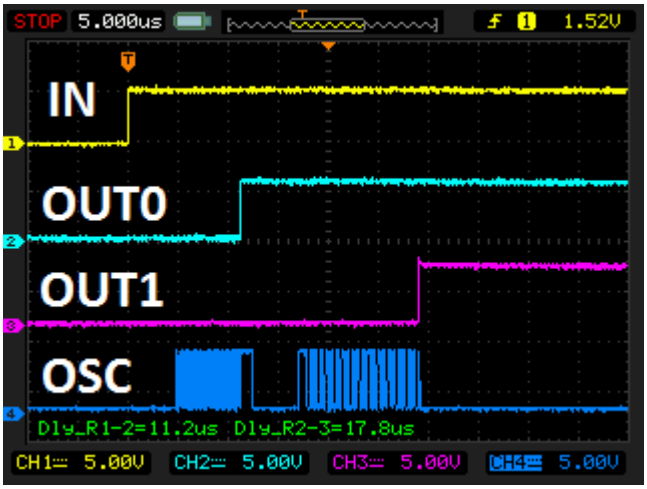


Channel 1 – 2-bit LUT0 output; Channel 2 – RC OSC output

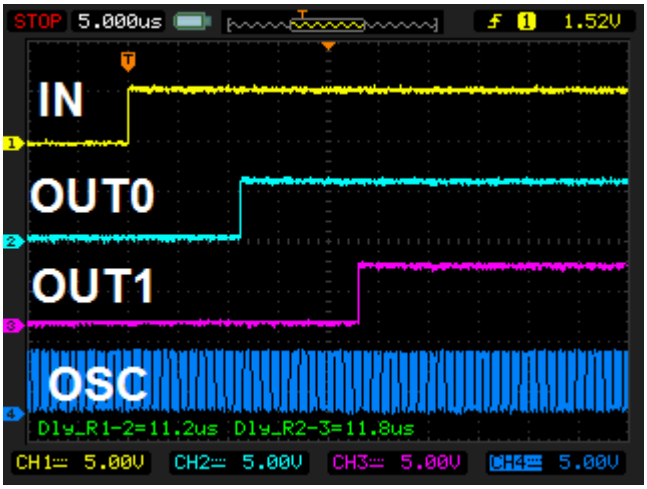
Such behavior will lead to substantial error in period calculations if the delay time is relatively small.

The same situation occurs while using two connected delays (all edge detect types except for a pair “Rising edge DLY – Falling edge DLY”).
In the following example, Delay0 and Delay1 are configured in the same way. However, Delay1 time is 17.8us instead of expected 11.3us (Delay0 time).



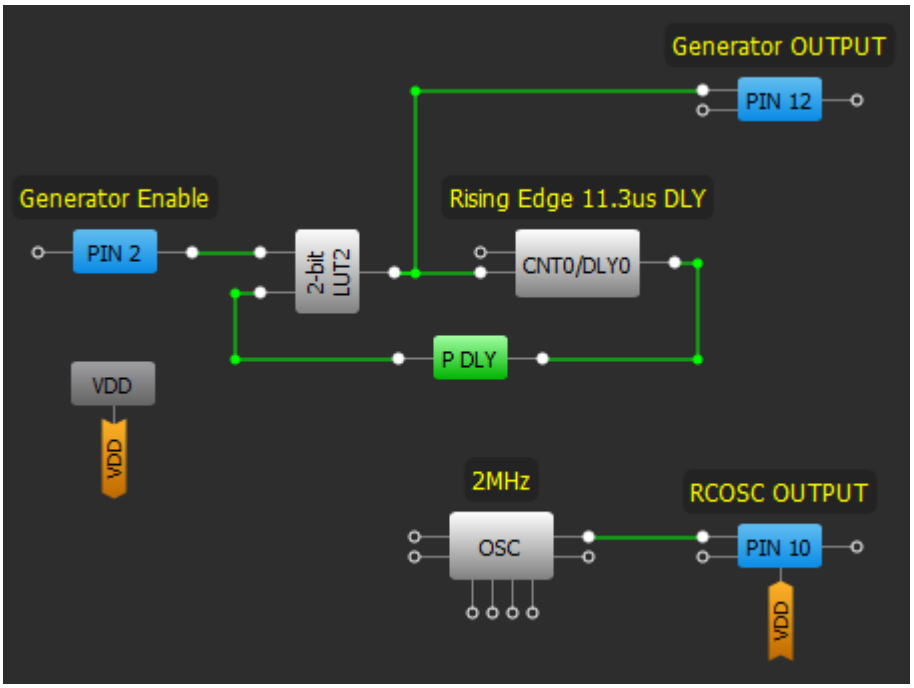


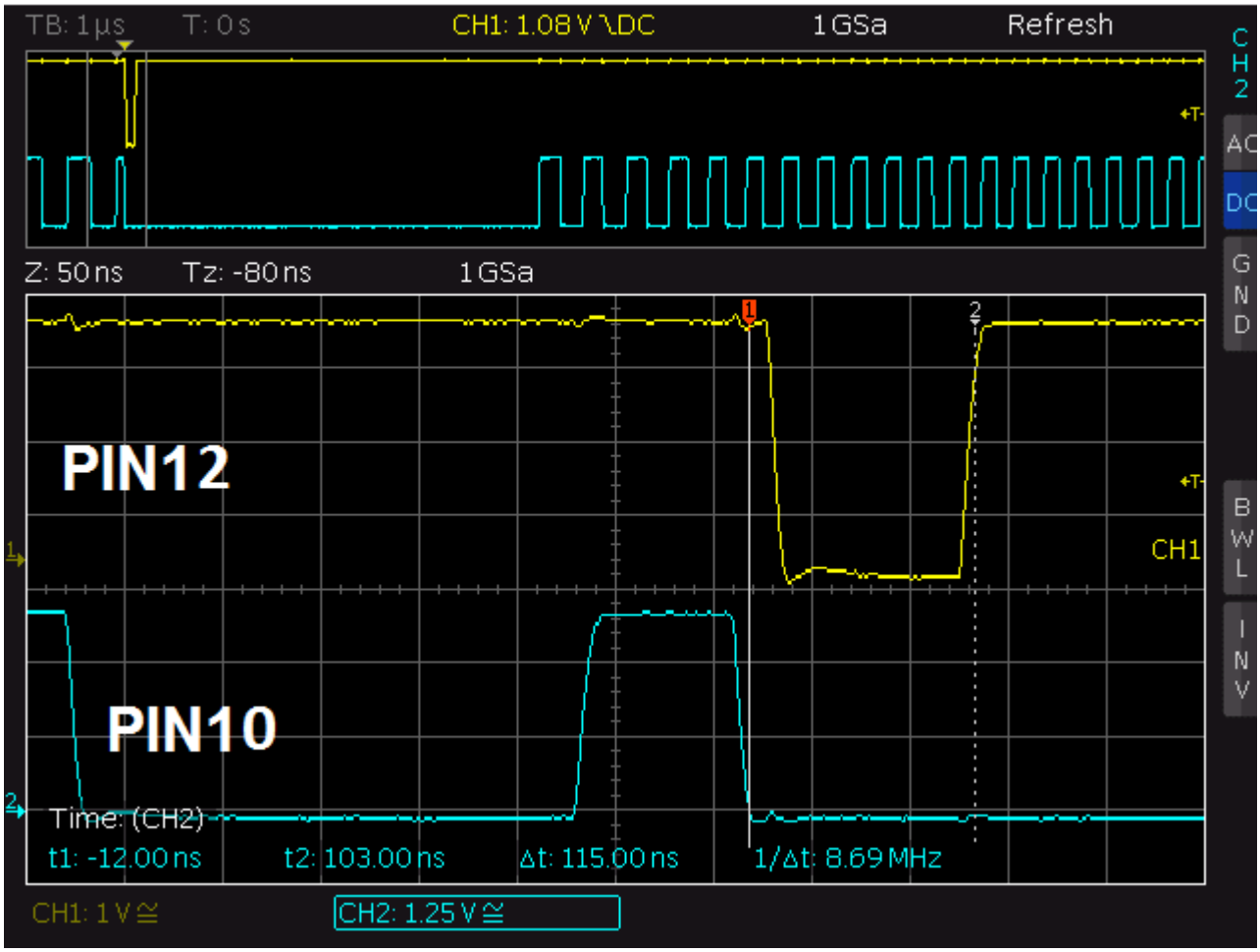
If there are some inner blocks which use RC OSC at the moment or RC OSC is forced power on when such error appears, RC OSC will be operational and delay value will be proper.



Workaround:

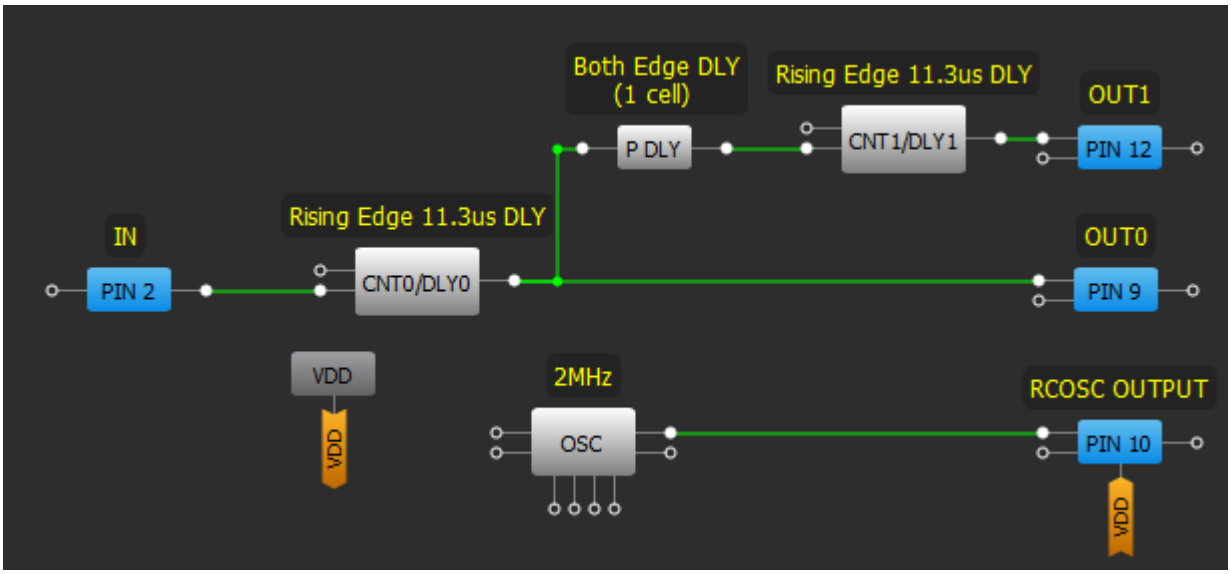
- In first case use block with longer propagation time.





Channel 1 – 2-bit LUT0 output; Channel 2 – RC OSC output

- Using two delays in series (except for a pair “Rising edge DLY – Falling edge DLY”) use one Filter cell or P DLY between delay blocks. Using LUTs won`t help in this case.



- Use the “Force power on” RC OSC power control option to make the RC OSC operate at all times.

ISSUE 2: Glitches on ACMP output
Functional Block Affected: ACMP

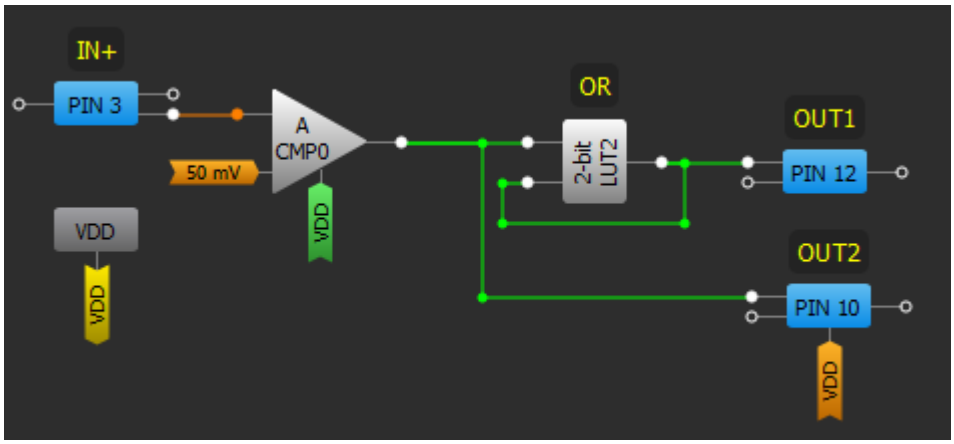
Description:

In some cases, ACMP may have short high-level glitches on its output (even if IN+ voltage is less than IN- voltage) after GreenPAK chip being powered up. Such cases may appear when using ACMP with Low Bandwidth mode enabled and Power Up is connected directly to the VDD.

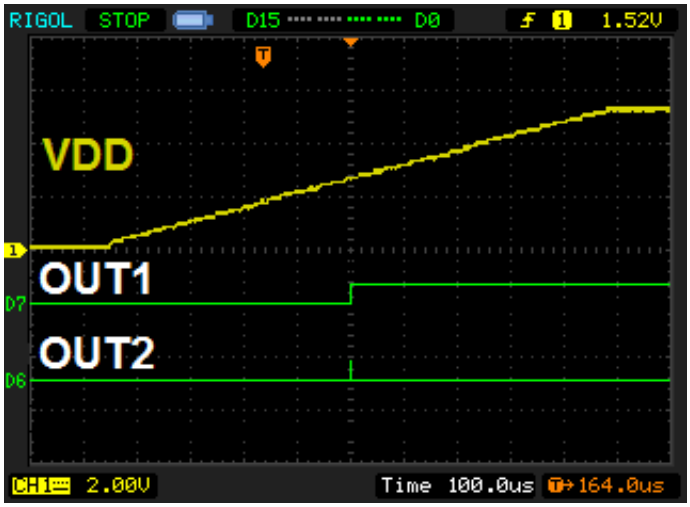
Conditions of glitches appearing are determined by IN- voltage, VDD value and VDD Ramp (see example tables below).

IN- Voltage, mV	VDD, V	VDD Ramp Time	Glitch presence
50	1.8	10 us	+
50	1.8	1 s	-
50	3.3	10 us	+
50	3.3	1 s	+
50	5.5	10 us	+
50	5.5	1 s	+
600	1.8	10 us	-
600	1.8	1 s	-
600	3.3	10 us	+
600	3.3	1 s	-
600	5.5	10 us	+
600	5.5	1 s	-
1200	1.8	10 us	-
1200	1.8	1 s	-
1200	3.3	10 us	-
1200	3.3	1 s	-
1200	5.5	10 us	+
1200	5.5	1 s	-

In order to detect such glitches, scheme with additional LUT was used. This LUT detects high level on ACMP output and stays high until chip powers down.

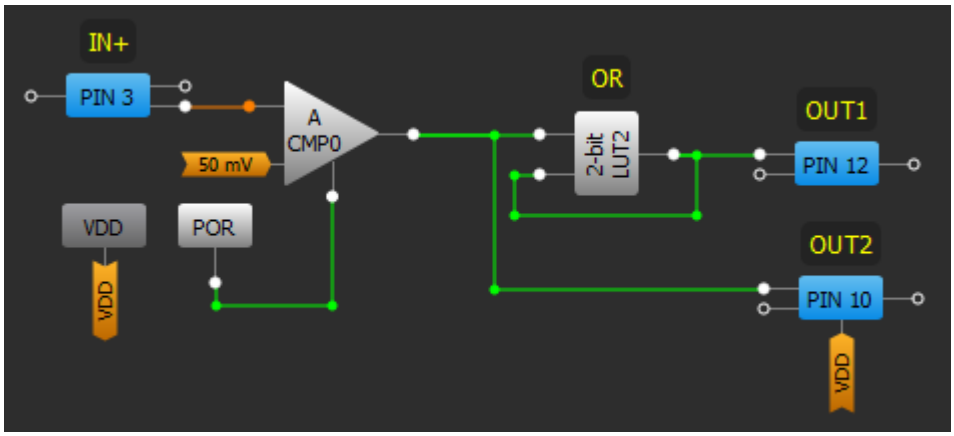


ACMP IN+ is connected to the Ground.



Workaround:

- Use POR block, connected to the ACMP`s Power Up pin. However, in this case ACMP will start working with low level output and will be able to go high only after POR goes high + ACMP power on time.

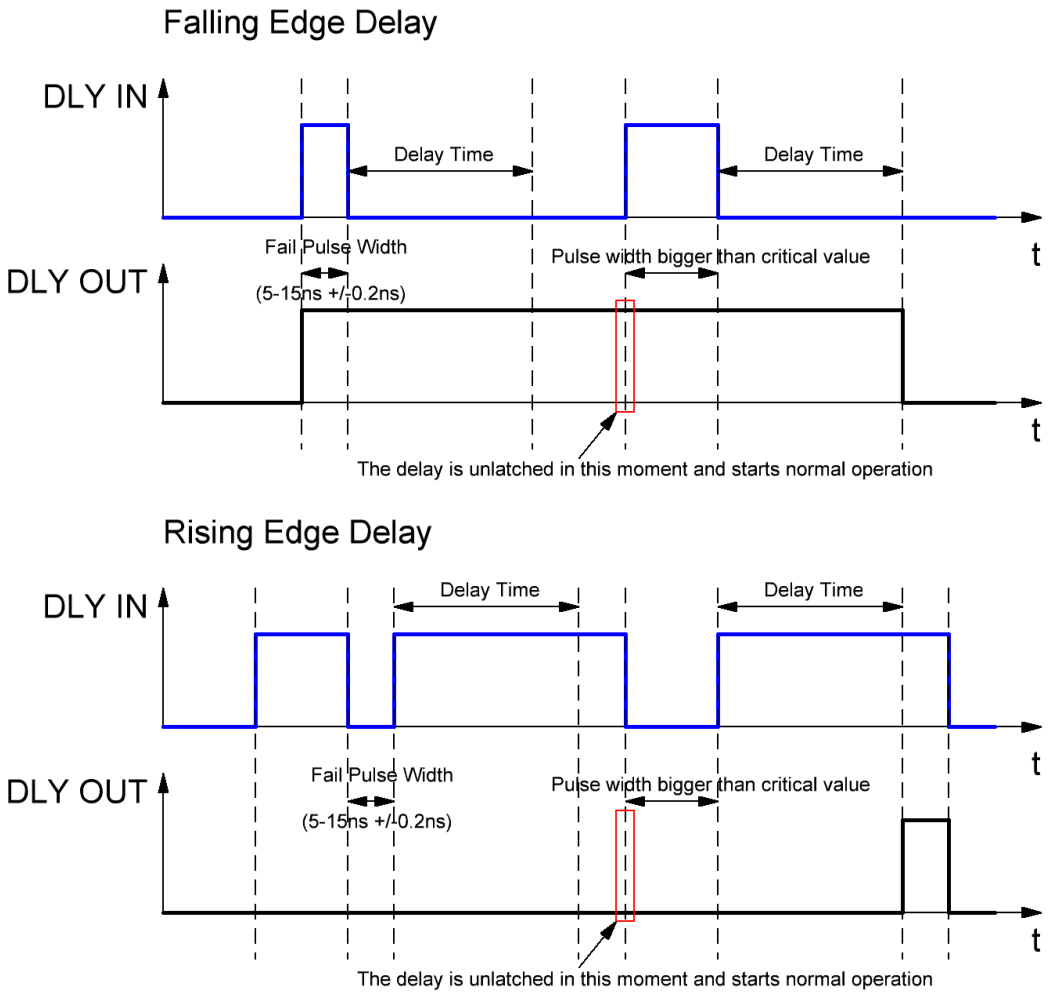


ISSUE 3: Delay Lock-up by a Short Pulse
Functional Block Affected: Delay

Description:

The delay output could be latched despite the input change when a short pulse is input. For example, if the delay cell is configured as a falling edge delay, the short pulse (see NOTE) appears on its input the delay cell output will switch from LOW to HIGH but may not switch from HIGH to LOW even after the delay time has passed.

NOTE: The pulse width varies from chip to chip and with different VDD voltage. It is in range of 5-15ns and in the window +/-0.2ns, so it should be very precise for issue happen.



Also, note that both edge delays do not have such issue.

Workaround:

- Use P DLY/FILTER block configured as a both edge delay or FILTER.

ISSUE 4: Device Damage by High Input Voltage on External Vref PIN of ACMP
Functional Block Affected: ACMPs

Description:

The device may be damaged by the voltage higher than 2V applied to IN- of ACMP as an external reference voltage.

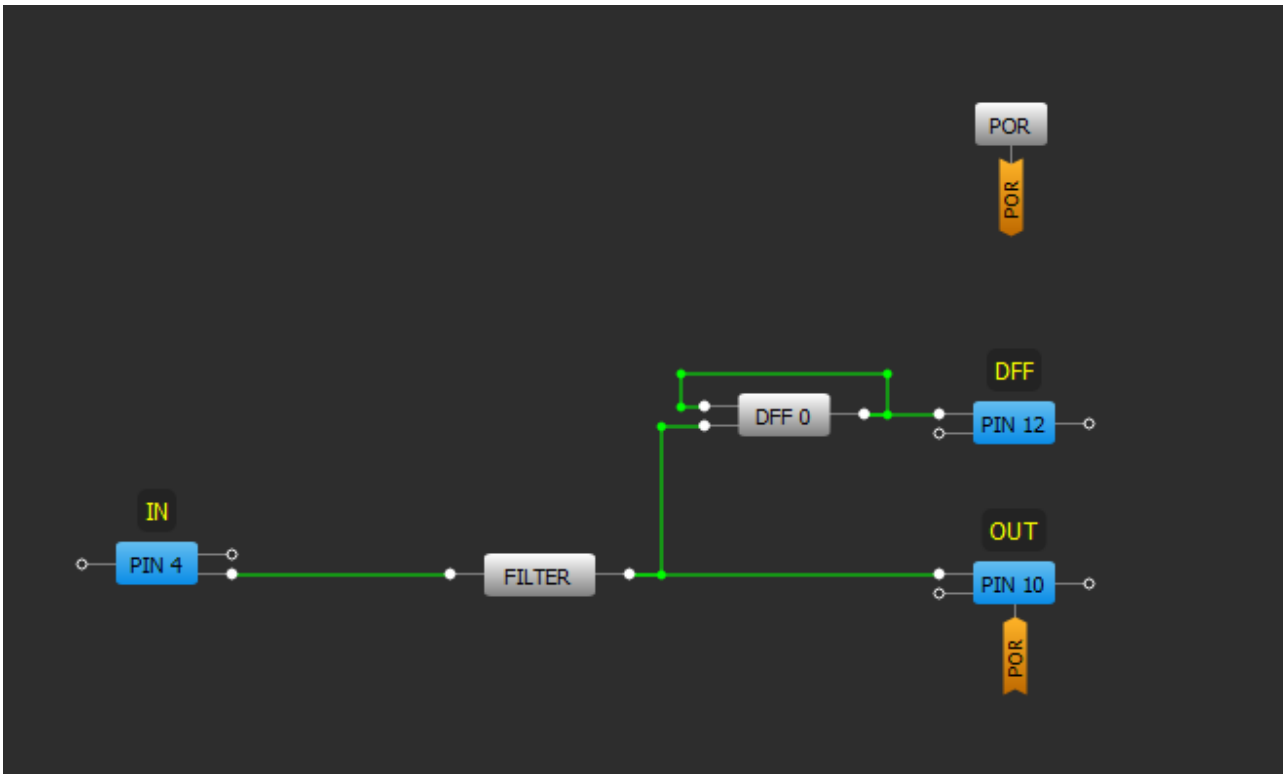
Workaround:

- There is no workaround to this issue, avoid applying more than 2V on IN- of ACMP used as external voltage reference.

ISSUE 5: FILTER cell does not filter out glitches
Functional Block Affected: FILTER

Description:

If clock type high frequency input comes in, the FILTER cell may not filter out it. There are several factors like input frequency, duty cycle and LOW duration in such signal that may lead to its passing through FILTER block.



Channel 1 (yellow/top line) – PIN#4 (IN)
Channel 2 (light blue/2nd line) – PIN#10 (OUT)
Channel 3 (magenta /3rd line) – PIN#12 (DFF)

1. Period is 60ns. Pulse width is 10ns DC=16.7% (Correct functionality)

2. Period is 60ns. Pulse width is 20ns DC = 33.3% (Incorrect functionality)

3. Period is 60ns. Pulse width is 30ns DC=50% (Incorrect functionality)

4. Period is 60ns. Pulse width is 40ns DC=66.67% (Correct functionality)

Workaround:

Currently there is no workaround for this issue. Filter block is good at filtering short spontaneous glitches. It is intended to be used in series connection before the delay cell to avoid its latching (see issue #5).

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