Introducing the Smallest Most Efficient High-Speed ADC for Connected Consumer SoCs

Adesto's ASIC & IP division has leveraged 15 years of design expertise in developing high-speed ADC architectures to create a state of the art family of SAR ADCs. The first in this series is a high-speed 160MS/s SAR ADC targeting highly integrated SoC's for consumer connected devices.

The S3ADS160M12BSM40LL provides class-leading energy efficiency of less than 31fJ whilst occupying less than 0.09mm^2 of silicon area. Utilising a 12-bit ADC core this converter delivers excellent dynamic linearity performance for all cellular modems and Wi-Fi connected devices, whilst delivering class leading power and area numbers. Currently available in SMIC 40nm, this single high-speed SAR ADC core consumes less than 6mW whilst utilising a mere 0.09mm^2 of silicon area. This core in 28nm will provide a class leading ADC that will consume less than 3mW, whilst using less than 0.06mm^2.

Choosing the Best High-Speed ADC for Your SoC

Consumer's voracious appetite for quick access mobile content is obligating the need for high-resolution, high-speed data converters in their mobile internet devices. Whether the transmission pipe is via cellular networks such as LTE or via local networks such as Wi-Fi, the end requirement for the data converter remains largely the same, that being higher bandwidth, higher speed, lower power and lower ownership costs that the consumer market can tolerate.

Key Consumer Market Requirements

The three key drivers that are pushing the evolution of data converter design are dynamic linearity over certain bandwidths, power consumption and silicon area. Presently, excellent dynamic linearity equivalent to greater than 10.2 ENOB is expected over bandwidths ranging from a few MHz to 80MHz, cellular LTE occupying the lower end, whilst Wi-Fi's 802.11ac occupies the higher-end. Typical power consumption budgets of less than 15mW are required, whilst silicon area utilization of the order of 0.15mm^2 and below is permitted. These are certainly tough requirements and only getting tougher!

What Metrics TO USE

A good figure of merit for comparing the relative performance of data convertors is the energy efficiency metric. This is given simply as:

$$\eta\text{energy} = \frac{\text{Power}}{2^{ENOB}\ X\ Fs}$$

with Power expressed in mW and Fs representing the sampling rate in Ms/s. In essence, this figure of merit captures the energy required per converted bit. The lower the number the better the relative performance. This metric, together with the silicon area used are arguably the two main critical factors that the SoC architect needs to consider when selecting the best in class data convertor for their application, once the input bandwidth requirement is met.

Architecture Choices

The choice of ADC architecture historically has tracked the end-user application. For example, industrial instrumentation sensing and audio have leveraged from the exceptionally high-precision, low speed over-sampled sigma-delta convertors. At the other end of the spectrum, where very high sampling rate and moderate to high resolutions that are typically required for data infrastructure, pipeline ADC architectures have dominated.

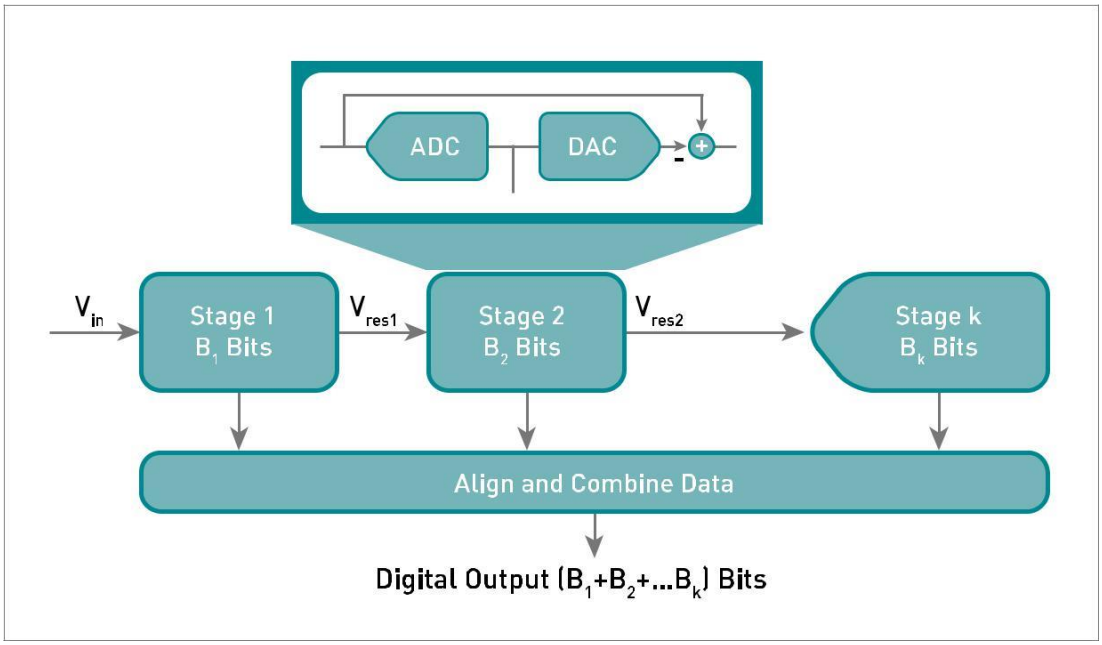

Figure 1. Pipeline ADC Block diagram

The highly-integrated consumer segment typically requires medium speed, medium precision data convertors. However, as discussed earlier the voracious appetite for larger bandwidth at speed is pushing the requirements into the same territory as the data infrastructure segment. Additionally, highly integrated consumer destined data converters have to deal with ever shrinking CMOS geometries from 65nm to 40nm to 28nm. Due to these geometries, mixed-signal design is moving towards big-Digital little-Analog circuit topologies, partially out of necessity, but also leveraging from the greater speed and integration possibilities at these deeper technology nodes. High-speed SAR ADC architecture matches this direction perfectly.

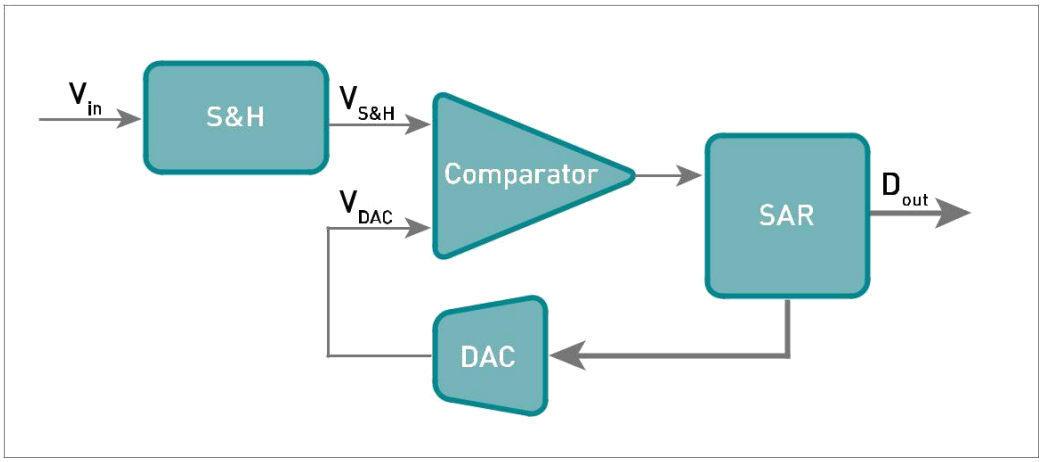

Figure 2. SAR ADC Block Diagram

Not alone will SAR based architecture bring more impressive power and area advantages but they will also decrease substantially the development effort by altering the design flow to become more digitally driven than analog driven (Big-D & little-A). This removes many of the inherent difficulties of designing efficient analog circuitry in the deep sub-micron technology nodes and therefore very substantially reduces the porting effort required to accommodate other technology nodes. This ultimately leads to a lower adoption risk, and quicker design cycle time.

Talk to us about how we can deliver these tiny, highly efficient, high-speed convertors to your consumer SoC.

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