DA6011 debugging guide

This application note is written to help engineers to debug PMIC related problems within the complex system built around Intel E6xx CPU.

Contents

Introduction

The DA6011 device is operating in a complex system build around the Intel CPU E6xx (formerly called Tunnel Creek) and the IOHubs. Due to this complexity and high assembly density it's difficult to determine the root cause for start-up problems.

There are at least three options to evaluate the system status:

1. Measure power domains and digital line status
2. SMBus access to DA6011
3. JTAG access to DA6011 and optionally CPU and SCH

I assume the reader has basic knowledge of DA6011 functionality and is already familiar with the SMBus and JTAG interface.

Measure power domains and digital line status

Since the power domains are powering up in different start-up states some power levels could be used to estimate the power transition state of the DA6011. In particular the buck converter outputs with their big inductivities could be easily identified. In the following picture

- The 1.2V BUCK signal identifies the SPD > S45 transition
- The 1.8V BUCK signal identifies the S45 > S3 transition
- The 1.05V BUCK signal identifies the S3 > S0 transition
- The CORE BUCK signal identifies the S0 state

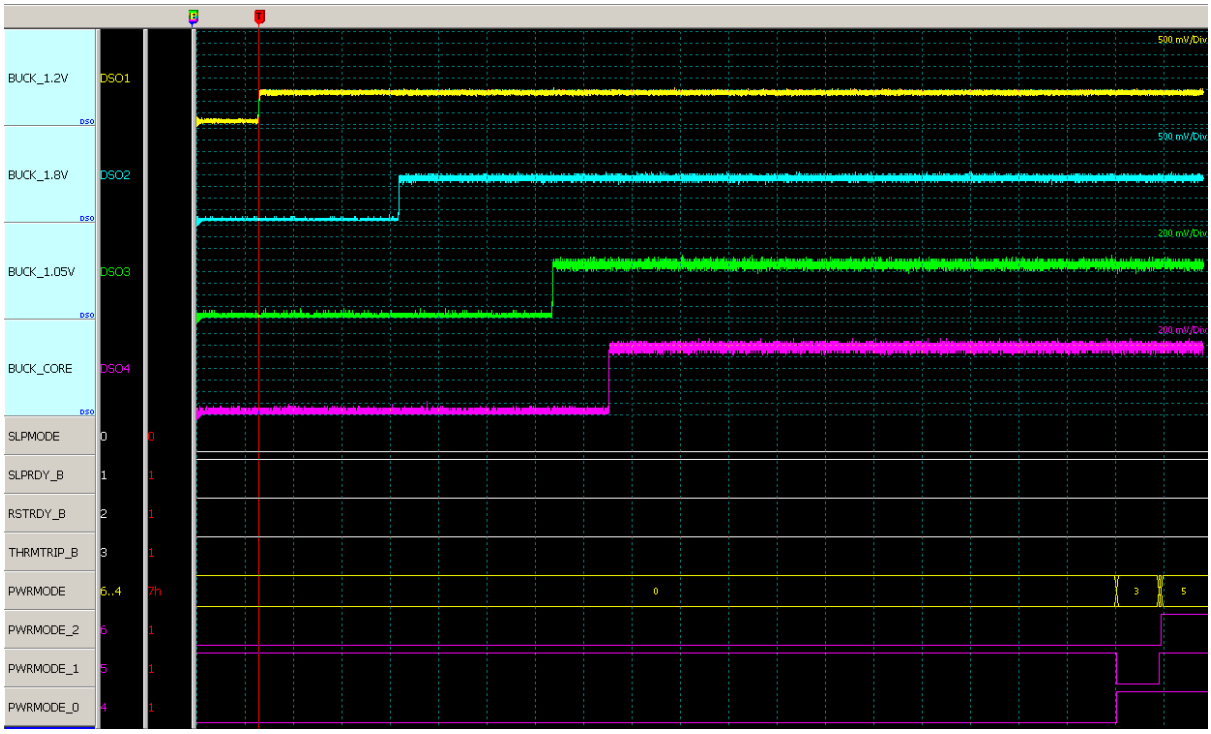


Figure 1 Voltage domain switch on timing during system start

I also captured the digital signals which could influence DA6011 start-up. SLPMODE, SLPRDY, RSTRDY and THRMTRIP are DA6011 inputs and should remain HIGH during the whole start-up phase. (SLPMODE & SLPRDY & RSTRDY) = LOW or THRMTRIP = LOW forces the DA6011 to immediately shut down (SPD mode).

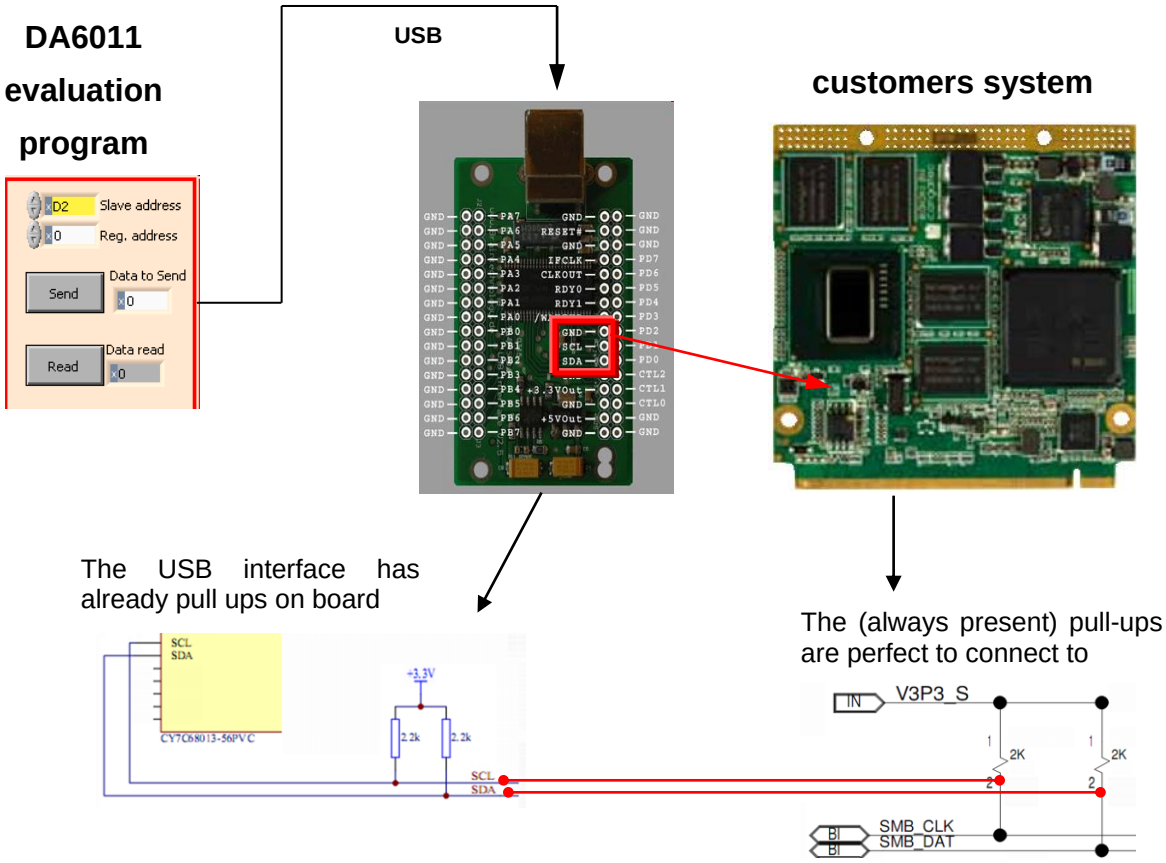
Due to a discrepancy with the Intel reference design the PRWMODE [0:2] signals could also create some start-up trouble. Intel specifies 60 Ω pull-ups to these signals which DA6011 can't drive. Since DA6011 has push-pull outputs you could just remove these pull-ups.

SMBus debug options

For general information about the SMBus and some practical hints please read

http://e2e.ti.com/cfs-filesystemfile.ashx/__key/CommunityServer.Components.PostAttachments/00.00.08.89.60/SMBus-made-simple_5F00_v5.pdf

We're using our USB module (which is part of the evaluation board) together with the eval application to communicate with DA6011 on the customer platform. Any other I2C interface, with some dispositions on the software, will work too. Our USB module doesn't support multi master setups but usually there is no or very less SMBus communication driven by E6xx. In any case you should check the bus activity before you connect your SMBus master.



The eval application is coded to respect the SMBus specific data count byte. If a different I2C interface is used the communication showed in the following examples should be implemented:

```
I2C display LA-data
s D2h a E4h a 01h a AAh a p              # write 0xAA to 0xE4
s D2h a FEh a 01h a p                    # set block count to 1
s D2h a E4h a s D3h a 01h a AAh n p       # read back register 0xE4
s D2h a E4h a 01h a 55h a p              # write 0x55 to 0xE4
s D2h a FEh a 01h a p                    # optional set block count to 1
s D2h a E4h a s D3h a 01h a 55h n         # read back register 0xE4
```

Figure 2 Single byte write and read sequences

```
I2C display LA-data
s D2h a E4h a 05h a 12h a 34h a 00h a 78h a 9Ah a p       # write 5 byte block (0x12, 0x34 ...) to 0xE4
s D2h a FEh a 05h a p                                    # set block count to 5
s D2h a E4h as D3h a 05h a 12h a 34h a 00h a 78h a 9Ah n  # read 5 byte block from 0xE4
```

Figure 3 Multiple bytes write and read sequence

Definitions:

s = Start condition; a = Acknowledge; n = no Acknowledge; p = Stop condition

E4h = Hex formatted data from master

45h = Hex formatted data from slave

Once connected, you're able to read and write the functional mode registers. If you enable the developer mode (SYSCSR (addr 0xD4) = 1), you get read and write access to the developer register, too.

By default the application is polling the visible registers and IO signal status twice a second. For manual SMBus access this could be disabled on the applications main page:

A very interesting register POCFSM (addr 0xD0) needs to be highlighted. It reflects the actual state machine status:

RegValue	Description
0x00	Init after POR
0x01	Initial OTP readout
0x02	Transition state from OTP readout to SPD
0x03	SPD (final state if failure event)
0x04	SPD to S45 handshake state
0x05	SPD to S45 state (transitional from SPD to S45)
0x06	S45 state: react on events
0x07	S45 to S3 handshake state
0x08	S45 to S3 state (transitional from S45 to S3)
0x09	S3 state: react on events
0x0A	S3 to S0 handshake state
0x0B	S3 to S0 state (transitional from S3 to S0)
0x0C	S0 state: react on events
0x0D	S0 to S3 handshake state
0x0E	S0 to S3 state (transitional from S0 to S3)
0x0F	S3 to S45 handshake state
0x10	S3 to S45 state (transitional from S3 to S45)
0x11	S45 to SPD handshake state
0x12	S45 to SPD state (transitional from S45 to SPD)
0x13	Warm reset

JTAG debug options

DA6011 provides an IEEE.1194.1-compliant JTAG interface. It needs five wires (TMS, TDI, TDO, TCK, GND) to connect the JTAG controller with DA6011 and the maximum TCK frequency is 10 MHz. Insure that DA6011 is directly connected to the JTAG master. If DA6011 is part of a scan chain you may face severe communication troubles because parts within the chain are not powered and will interrupt the chain.

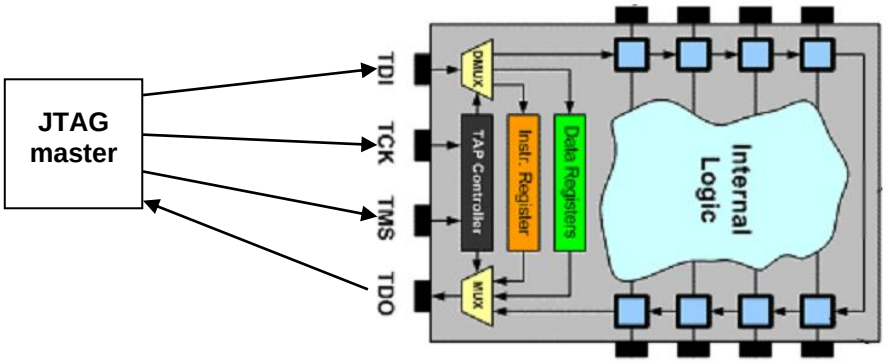


Figure 4 Typical JTAG connection

We've evaluated two controller options. A professional tool bought from XJTAG (http://www.xjtag.com/) which consists of an interface XJLink and the software XJAnalyser. In combination with the BSLD file (which we provide) you easily get a nice graphical signal overview.

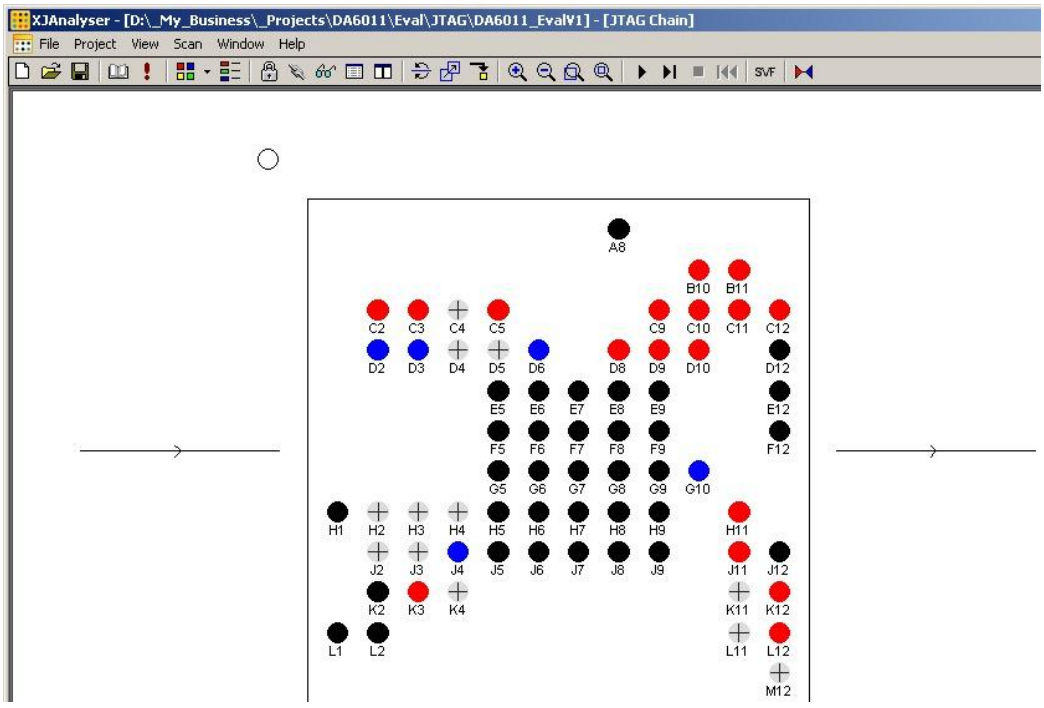


Figure 5 XJAnayzer in the signal monitoring mode

For cost reduction but also to increase the functionality, we've designed an own JTAG master into our new USB-Interface (ULI). It enables us to control the power state but also to capture the available signals in a Logic Analyzer like way. For detailed information please read the DA6011_JTAG-Monitor_User Guide (UM-PM-001).

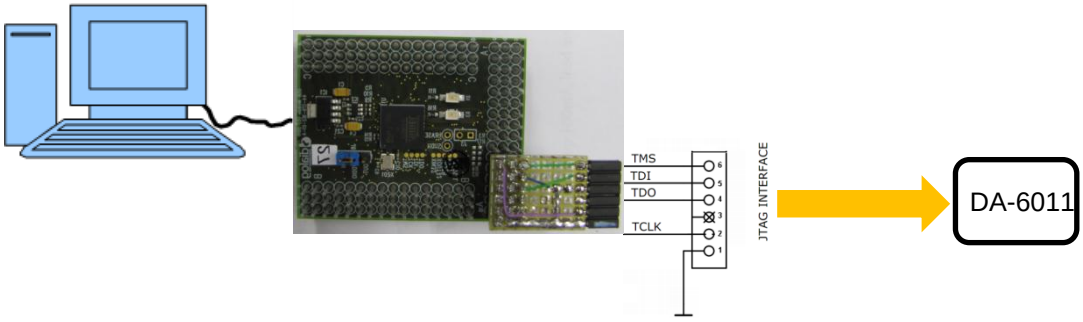


Figure 6 Dialog USB-interface connting to DA6011 JTAG

The JTAG-Monitor application has two tabs offering two different possibilities to access DA6011.

Interactive page

The interactive page serves as a manual, slow interactive GUI to monitor the signals.

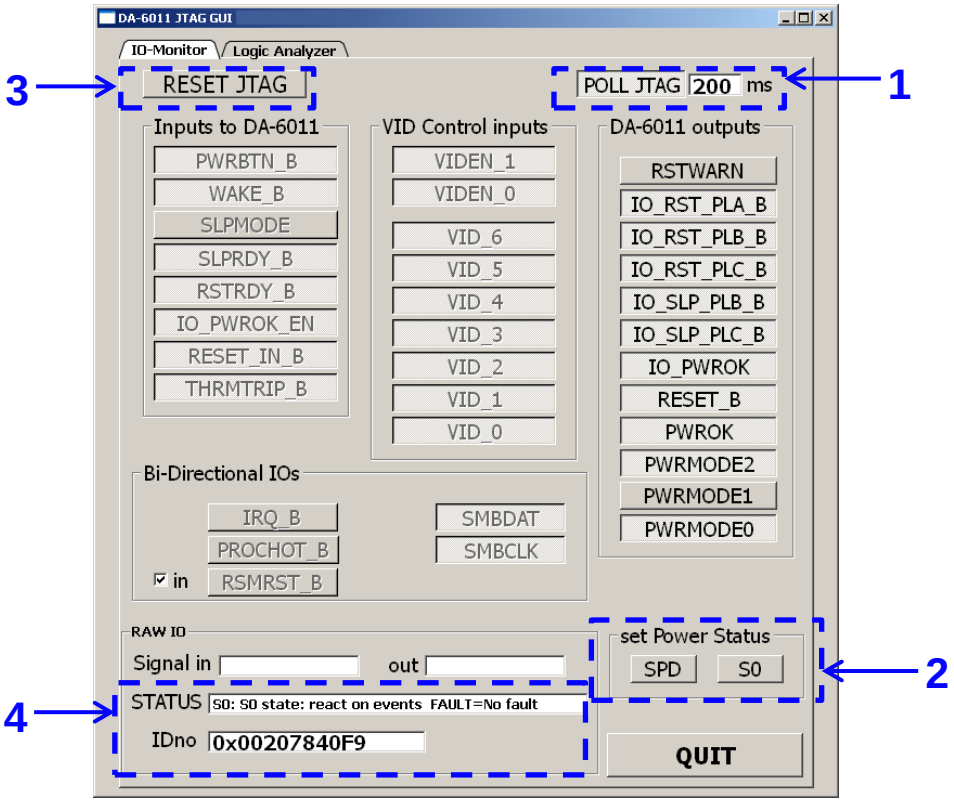


Figure 7 Interactive page

Block 1: Button to start signal polling and a field to specify the polling rate.

Block 2: Buttons to force the DA6011 into S0 or SPD mode. DA6011 is isolated from the input signals and therefore won't respect any external signals which could hint it to change the mode.

Block 3: Button to optionally reset the USB-JTAG interface.

Block 4: Info area reflecting the identification number and DA6011 working mode.

Logic analyzer page

The logic analyzer page enables the user to run the JTAG interface in a logic analyzer mode. This mode is only monitoring DA6011 signals and its intention is to capture e.g. system start-up. A logic analyzer application was modified to display the captured data. It is started and controlled from this page. The captured data is transferred between the applications through files.

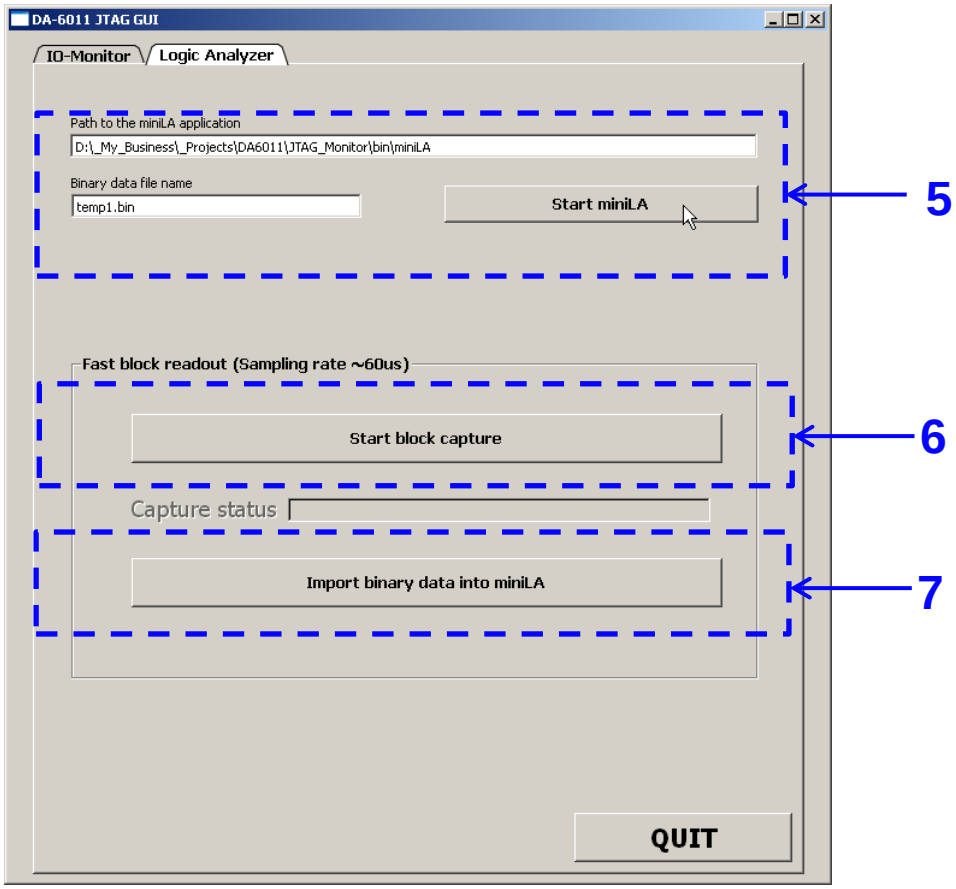


Figure 8 Logic analyzer page

Block 5: To start the logic analyzer press the "Start miniLA" button. It's possible to store the captured data into different binary files by changing the binary file`s name.

Block 6: The JTAG capturing is started and stopped with this button and the capturing status is displayed in the "Capture status" field.

Block 7: Once the capturing is finished this button starts the data processing, storing and transferring into the LA.

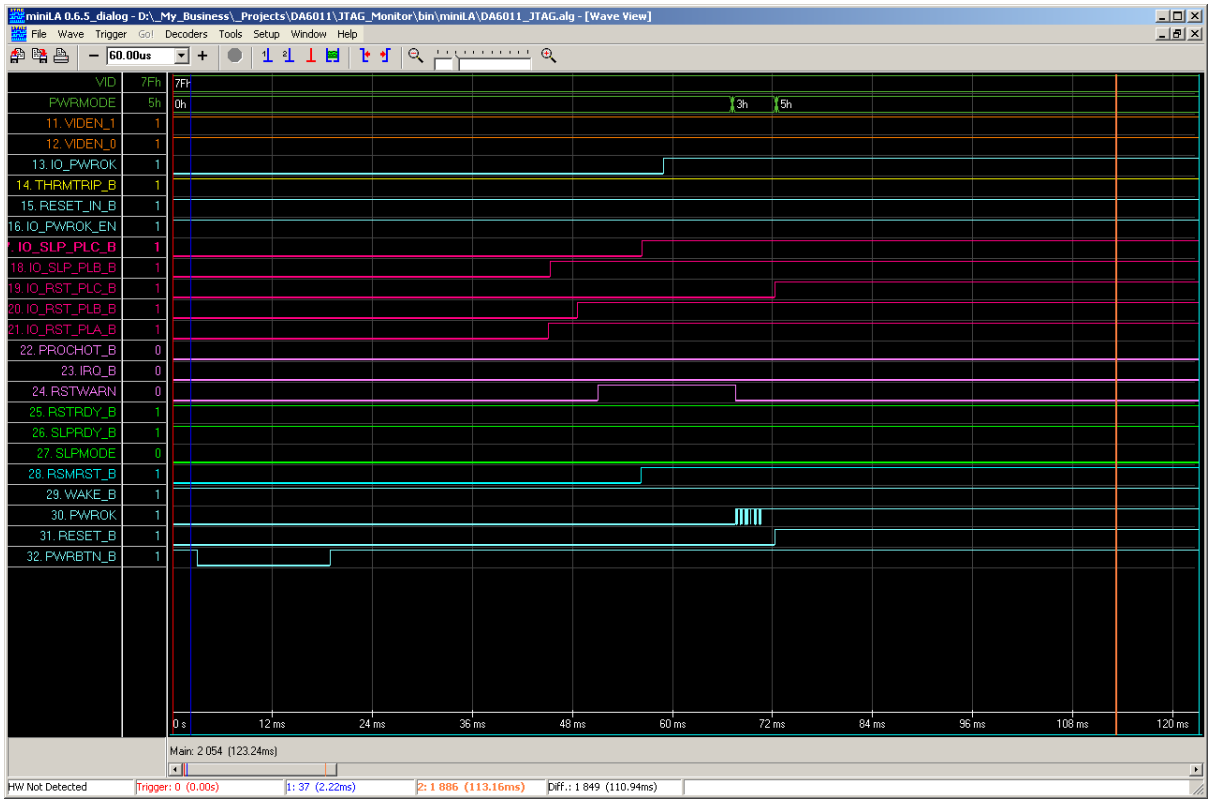


Figure 9 LA showing a captured start-up sequence

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