A Case Study - RF ASIC validation of a satellite transceiver

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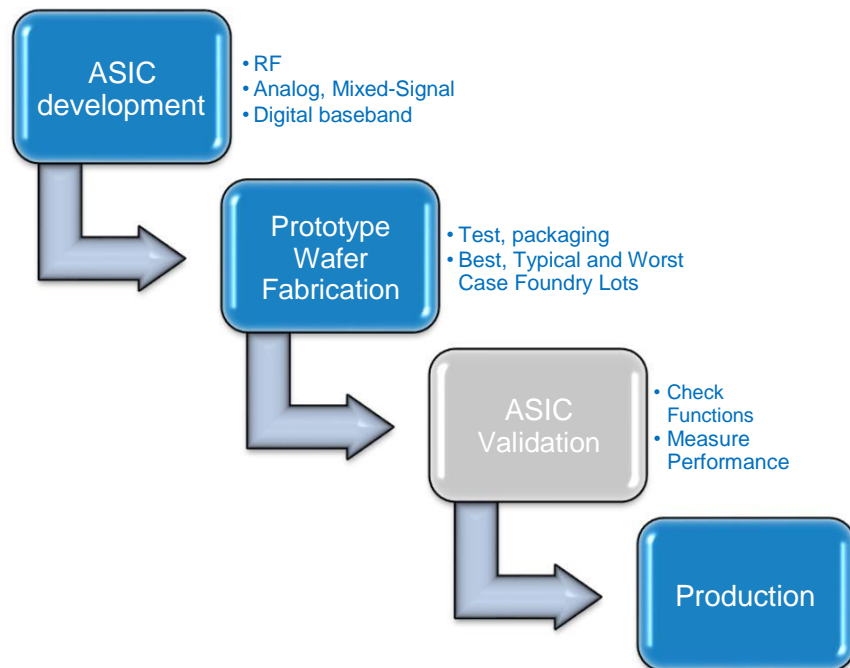S3 Semiconductors

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Abstract

ASIC validation in the RF world comes with its own set of hurdles and challenges, with high quality lab equipment, experience and know-how essential. A recently completed RF sub-system validation at S3 Semiconductors is presented in the form of a case study of the execution. The validation PCB design focussed on impedance matching and shielding RF signals from noise sources. We built up an efficient, automated test harness based on LabVIEW, MATLAB and python. This unified test framework facilitated instrument set-up, test-case running, data collection, traceability, plotting of measurements, waveform generation and analysis.

Planning for Validation

This is a case study of the validation of a complex RF subsystem, carried out by S3 Semiconductors. It suggests some best practices and approaches to adopt.

A specialized S3 Semiconductors ASIC RF development team designed a complex satellite transceiver, for use in handsets (phones) and modems. Die samples were fabricated in three lots (Best, Typical and Worst Case) by TSMC in a 0.18µm RF CMOS process, which were packaged and tested. Approximately 100 of these samples were used to validate the IC design's functionality and performance.

ASIC development
- RF
- Analog, Mixed-Signal
- Digital baseband

Prototype Wafer Fabrication
- Test, packaging
- Best, Typical and Worst Case Foundry Lots

ASIC Validation
- Check Functions
- Measure Performance

Production

Make a Plan

It all starts with a clear black box specification, on which a testing strategy can be built. It must include individual, numbered, test items with their pass/fail criteria, usually in the form of an RF parameter, e.g. Phase Noise, ACPR. The aim is to build and execute a minimum set of tests to cover all these identified test items. In our case, we had 194 test items covered by 68 different tests.

Have the right team

The correct range of disciplines is essential.

Skilled RF board designers, experienced with the manufacture and assembly of custom validation boards, experienced engineers with DSP and wide-ranging programming experience and of course, experienced RF engineers.

Build up the lab environment

At RF frequencies assume that expensive, high-end lab equipment is an essential requirement. How many benches/stations are needed? Our recommendation is at least one per validation engineer. We split the validation team up into Support, PLL/SYNTH, TX, RX, and Auxiliary Functions.
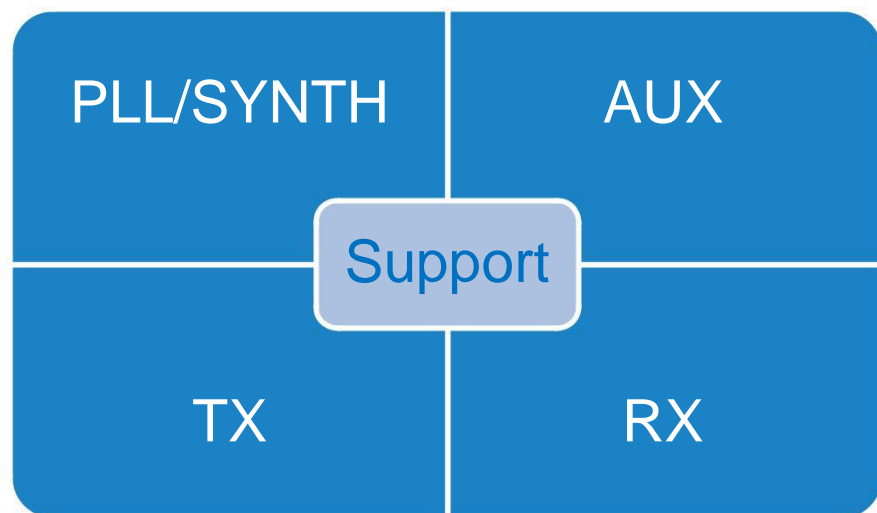

Figure 1: Validation Team structure

The support engineers are crucial to the validation process. They provide the assembled validation boards, software drivers and test harness framework.

The RF Sub-system

The system or device under test (DUT) is half-duplex, where transmit and receive operate in separate time-slots. Both receive channels (and hence both PLLs) may be active at the same time, when one channel is receiving a signal, and the other is in search mode.
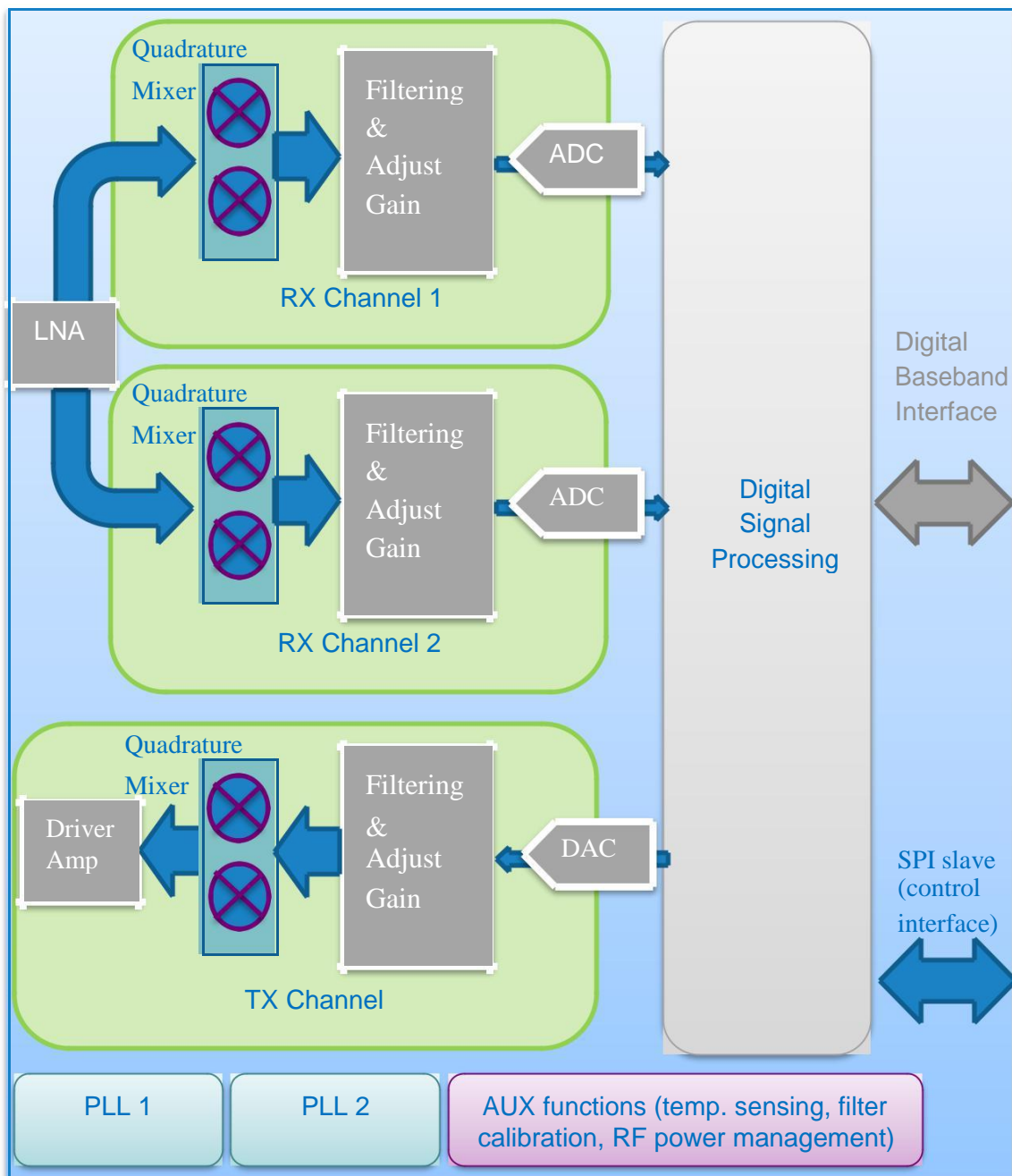

Figure 2: RF sub-system under test

Making it happen

Board Design

"Protect and shield the RF signals from noise"

The number one rule here is to protect and shield the RF signals from noise. With this in mind, we designed a separate RF daughter board and interconnection mother board. This step alone keeps the majority of noisy digital clocks and signals away from the RF section.

Careful routing and/or shielding of RF signals is critical to protect from any potential noise sources. Particular attention must be paid to low-power RF signals, as they are significantly more susceptible to noise than high-power signals.

High spec accessories (connectors, cables, terminators, couplers, adapters, attenuators) are a wise investment, as poor accessories can degrade the signal significantly. Spec items to look out for are VSWR, return loss, insertion loss over the frequency range of interest. Other considerations are connector type, e.g. N-type versus SMA, right angle versus straight.

Test points must be inserted at various points (output of TX, input to RX etc.), bearing in mind impedance matching at all stages.
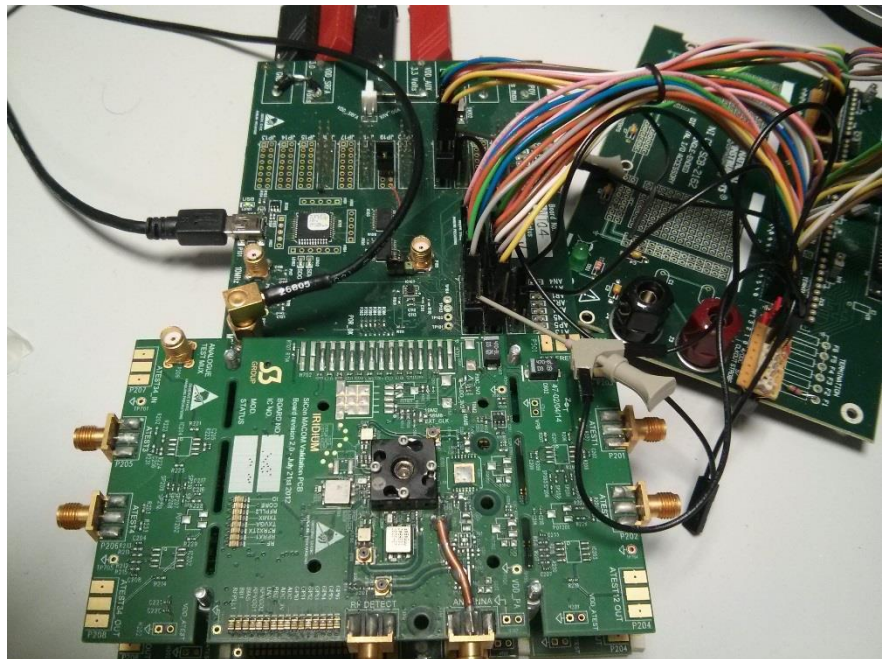

Figure 3: RF board and interconnection boards

Software Infrastructure

Develop the device drivers, both SPI control interface and digital signal interface. In our case, we created a LabVIEW GUI to control the register address space, with SPI read and write sub-functions driving a USB-to-SPI IC on board. The GUI was invaluable for debug, as 'ease-of-visualization' of the address space is critical whilst debugging test cases and bench set-up. The GUI was also fully re-usable in an automated mode within the test harness.

The interface at the digital baseband was driven with realistic waveform bursts transmitted via a digital pattern generator. The waveforms were MATLAB-generated, with randomized payloads. The full suite of test-stimulus waveforms consisted of QPSK, 8PSK, 16APSK in a variety of digital baseband bit-rates.

Connected to the digital baseband interface's receiver was a Logic Analyser, which captured the burst data at the positive clock edge. The captured data was analysed in MATLAB with a suite of specialized scripts, particular to each test case (e.g. Noise Figure, EVM).

Python (including libraries such as numpy, scipy, matplotlib, pylab, math) was also used extensively for digital signal processing functions such as waveform generation, data analysis etc.

LabVIEW Test Harness Framework

A suite of LabVIEW functions was developed for an array of test equipment, including Network Analyser, RF signal generator, RF vector signal analyser, Logic Analyser, Pattern Generator, Temperature forcer, DC voltage source. These functions encapsulate the device drivers to provide setup, control and measurement services, and as such provide building blocks to the test cases.

> "Ease-of-visualization of the address space is critical whilst debugging test cases and bench set-up"

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by Adesto

A LabVIEW test harness was developed to provide a unified framework for running each test.
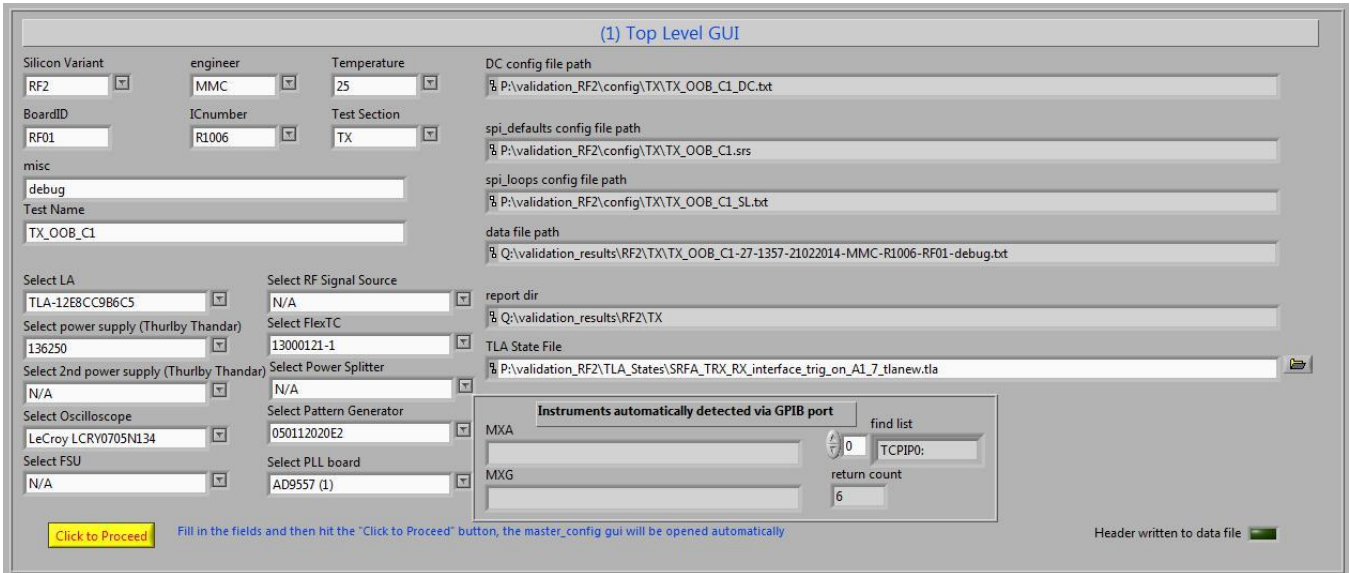

Figure 4: LabVIEW test harness

Each test result/measurement file has the same format, right down to the header. This header information provides traceability, which is critical for the integrity of the validation.
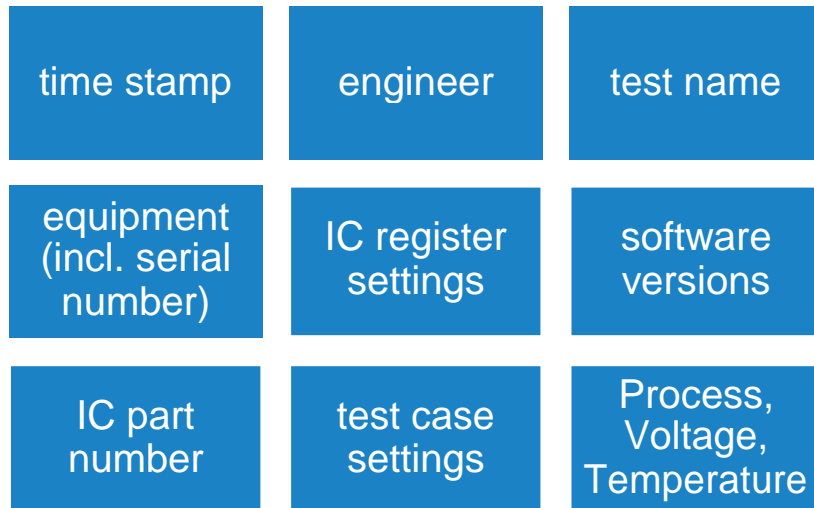

Figure 5: Results file header information

"Visual analysis of the measured data goes hand in hand with the daily data collection"

We used CSV format for all of our results files, as it is easily imported into visual data analysis tools (e.g. MS Excel). Visual analysis of the measured data goes hand-in-hand with the daily data collection. Python is also a pragmatic method of producing good plots, particularly at the stage where test automation has matured. We used the Python Pandas package.
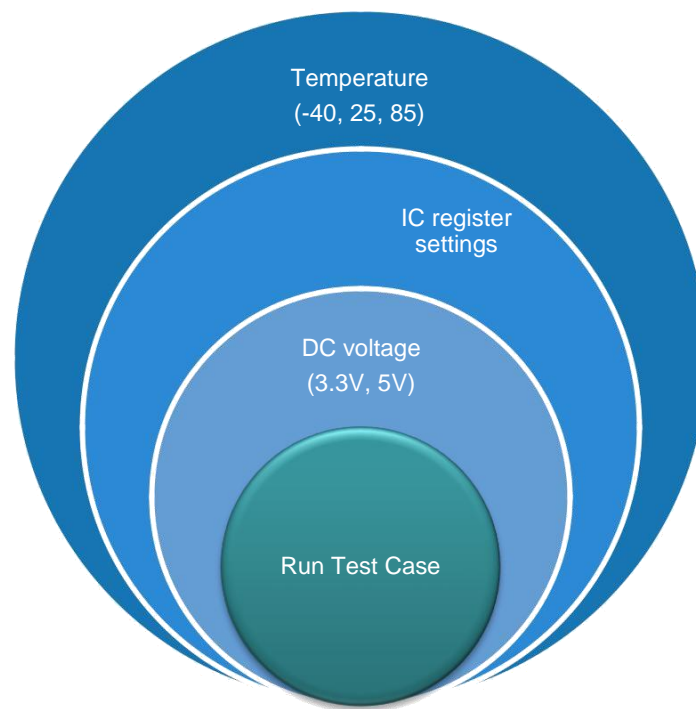
Figure 6: Nested test loops

The test harness facilitates the re-running of the core test case in nested loops with different settings [DC voltage, IC settings, Temperature], and amalgamating all the measurement data into a single results file.

In our experience, the test harness gives significant productivity gains, providing a predictable and deterministic process. It not only facilitates intra-team collaboration, but also promotes the reliability of the data collection.

This deterministic test process facilitates significant automation of data visualization, graphing and plotting, which is vital for catching anomalies and debug.

Problems encountered and approaches to solution

As in any engineering project, there are some hiccups and pitfalls to overcome.

Over the course of the validation, we found that individual validation boards were malfunctioning, and that this was happening more frequently than expected. To make matters worse, debug of this problem was difficult because each faulty board had a different defect.

The initial suspected source of the problem was poor handling practised by the validation engineers, however on review of the process it was confirmed that due care was being exercised by all and engineers were already following our ESD handling procedures.

The manufacture/assembly process was also investigated as a potential source however, our incoming inspection process proved that this was not the culprit. The screening process for incoming boards, which included a visual inspection, as well as a suite of automated screening tests to quickly test the core functions, confirmed this was not the source.

A review of the validation and bench setup, highlighted the addition of a new piece of equipment, a temperature forcing system. This was the only change to a setup that had been proven reliable in the past. On closer examination of the data generated by the test suite, made easy through use of standard report generation and UI discussed earlier, we discovered that temperature cycling the test boards over a short time period, was stressing the board integrity as it was swept from -40°, through 25° and 85°.

Slowing the temperature cycling right down, proved very successful at fixing the problem. We then set about finding the balance of temperature cycle time that was fast enough to complete testing in a desired timeframe, while also ensuring the integrity of the test boards.

A solid systematic approach to running test cases, collecting and reporting data, was fundamental to debugging the problem quickly and efficiently.

Understanding the measurements

Attention must be paid to every link in the chain!

Calibrate the equipment

- All measurement equipment *must* be calibrated to ensure the integrity of the measurements

Cable Loss

- Measure the cable loss and factor it in to the measurements

Impedance Mismatch

- Eliminate or minimize impedance mismatch

Use high quality attenuators, terminators, adapters and cables

- High quality attenuators can improve VSWR at the load

Understand the measurement equipment

- Use the higher level built-in functions of the equipment where appropriate
- Provide training to the engineering team on new pieces of equipment

Conclusion

For a successful validation program, let's start with the fundamentals (getting the basics right!)

- Experienced team with the right competencies and disciplines
- High quality RF lab equipment essential ($$)
- Debug ports designed in to ASIC
- Unified test approach (use of LabVIEW function blocks, LabVIEW test harness etc.)
- Time-stamped results files, proper paper trail (Engineer, date, equipment, IC settings used etc.).

It is advantageous to have ready access to the RF ASIC design team, with their extensive knowledge of the design. If a quick design re-spin of the validation boards is necessary, then turn-around time and a good tie-in with 3rd party board manufacture and assembly houses is crucial.

Our unified LabVIEW test framework awards great gains in productivity, as it promotes same look-and-feel of the test case suite and expedites cloning/adjustments of test cases. The test harness also facilitates test loops (re-runs) for temp, DC voltage, programmed IC settings, as well as providing a unified approach to CSV file output, which is essential for data analysis and results tracking. We used MS Excel for analysis of data and fine-looking plots in final report.

About S3semi

S3semi is a wholly owned division of Adesto Technologies. S3semi designs advanced mixed signal chips and manages every aspect of supplying production devices to its customers using some of the world's most advanced semiconductor production facilities. With more than 20 years' experience designing advanced analog and digital circuitry for hundreds of customers in every major region.

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