

# Application Note

## Extending the SLG59M1693C's Maximum Operating Current Range

AN-CM-240

### Abstract

*This application note shows how to extend the SLG59M1693C's maximum operating current range.*

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**Extending the SLG59M1693C’s Maximum Operating Current Range**

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**Extending the SLG59M1693C's Maximum Operating Current Range****1 Terms and Definitions**

IPS                      Integrated Power Switch

**2 References**

[1] SLG59M1693C, Datasheet, Dialog Semiconductor

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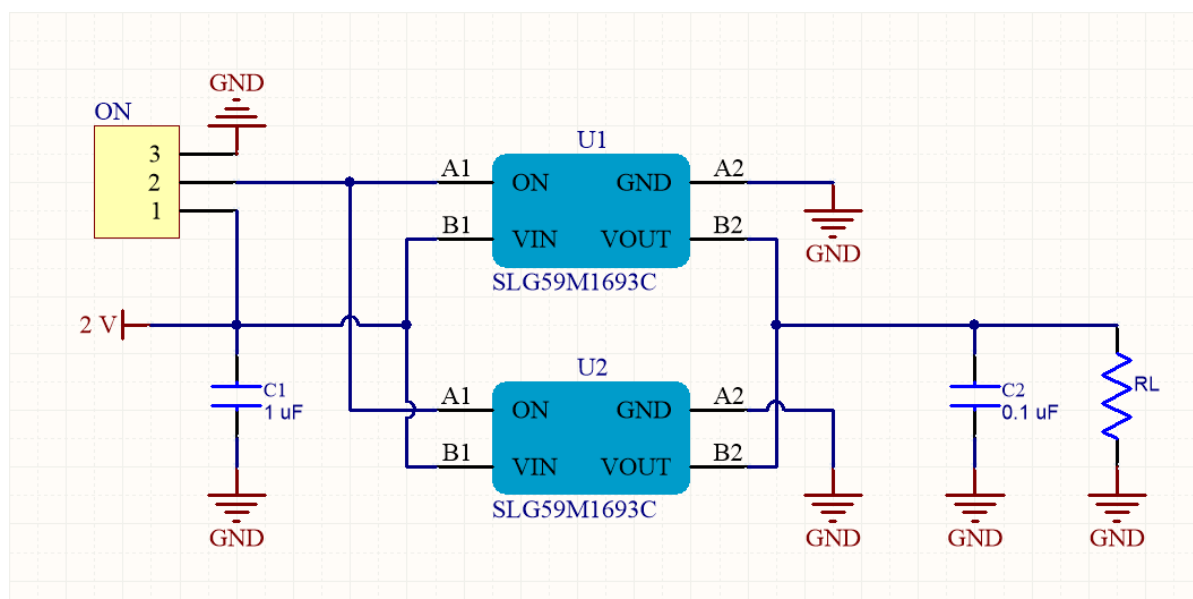
## Extending the SLG59M1693C's Maximum Operating Current Range

### 3 Introduction

Some applications require an IPS to deliver currents higher than 1 A. One way to address this requirement is to use an integrated power switch with higher current capability. However, such a part may occupy more PCB area or consume more power than optimal for the desired current rating. Another way to obtain higher current capability is to parallel two IPSs.

### 4 Using Two SLG59M1693Cs in Parallel

Parallel arrangement (Figure 1) divides the current between each IPS accordingly to its  $R_{DS(on)}$ .



**Figure 1: Schematic Layout of Connecting Two SLG59M1693C IPSs in Parallel**

Using two IPSs in parallel lowers the overall  $R_{DS(on)}$  while maintaining low current consumption when ON, for any applications up to 2 A. A typical  $R_{DS(on)}$  vs. Temperature and  $V_{IN}$  for this configuration is illustrated in Figure 2.

## Extending the SLG59M1693C's Maximum Operating Current Range

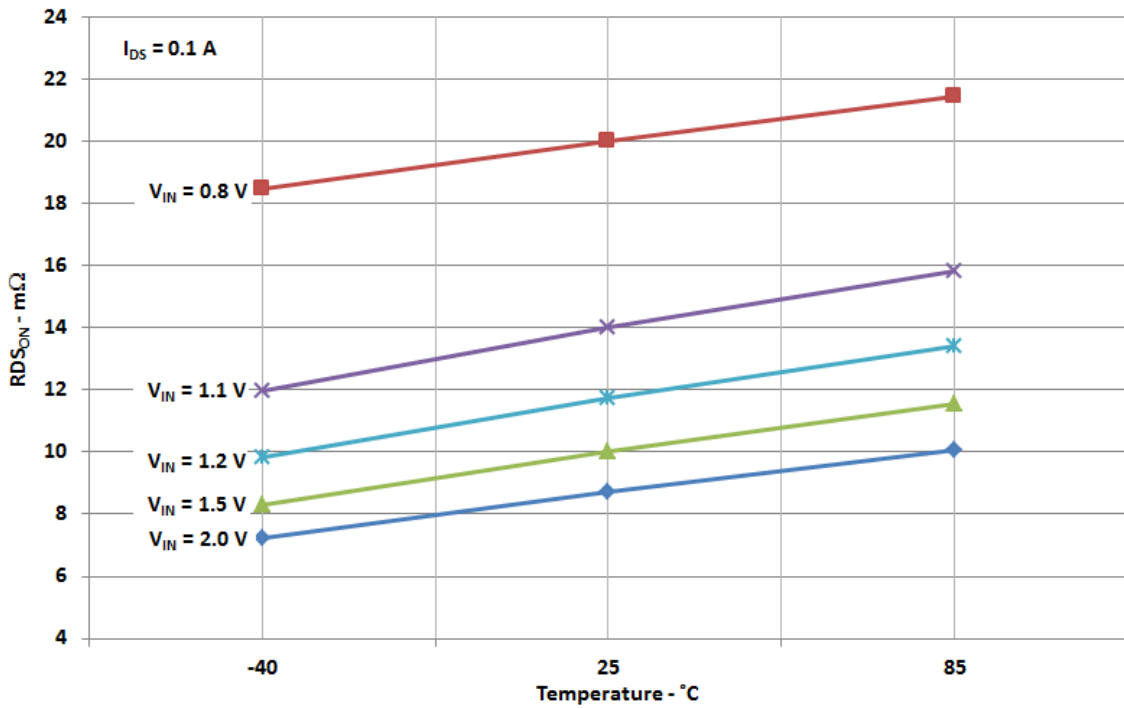


Figure 2: RDS<sub>ON</sub> vs. Temperature and V<sub>IN</sub>

All PCB traces have the elements of resistance, capacitance and inductance. If there were a difference in path length from the voltage source to the IPSs pads, this delta trace length would create a current imbalance. In this case, the PCB layout should be designed properly to minimize parasitic impedance and especially parasitic inductance on V<sub>IN</sub> and V<sub>OUT</sub> pins. Excess trace inductance may cause a delay effect during on/off operation. Figure 3 shows a recommended PCB layout for applications using two SLG59M1693Cs in parallel.

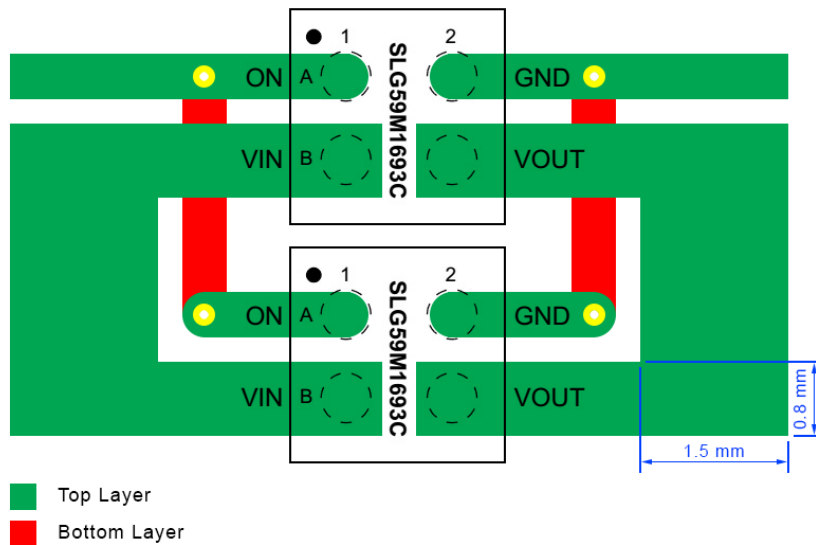


Figure 3: PCB Layout for Using SLG59M1693C in Parallel

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Typical operational waveforms of this two IPS solution are illustrated in Figure 4 and Figure 5.

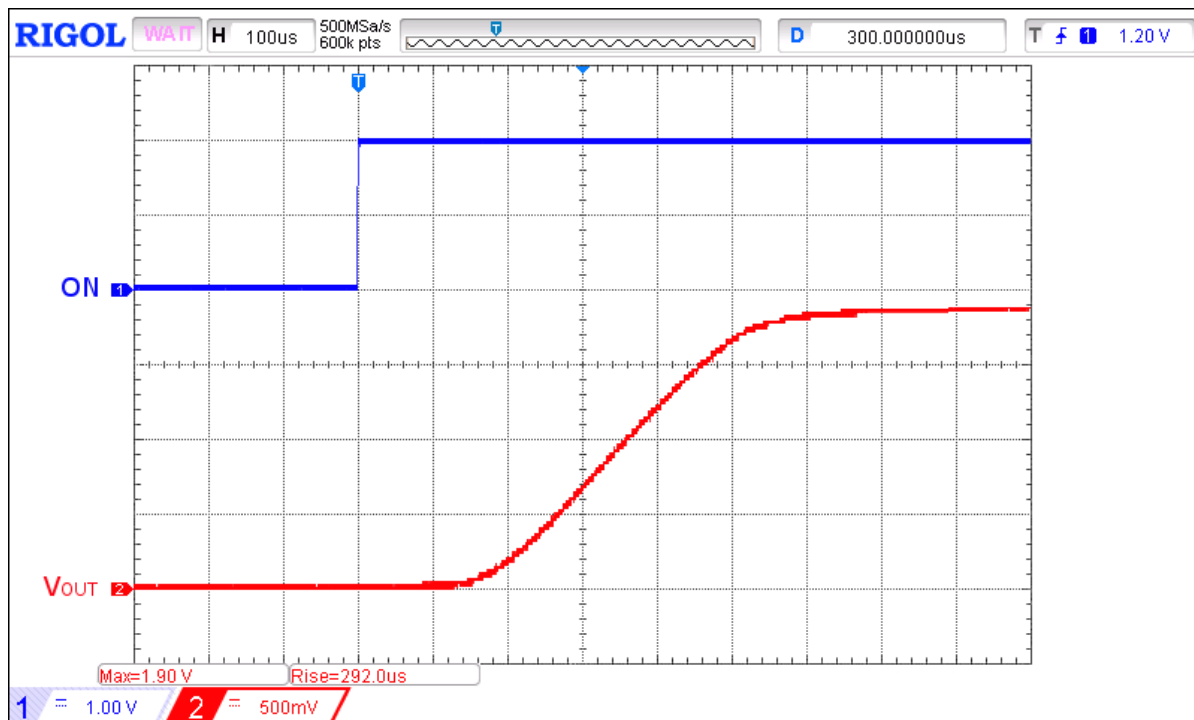


Figure 4: Turn on Operation Waveform for VIN = 2 V, CLOAD = 0.1 μF, RLOAD = 1 Ω

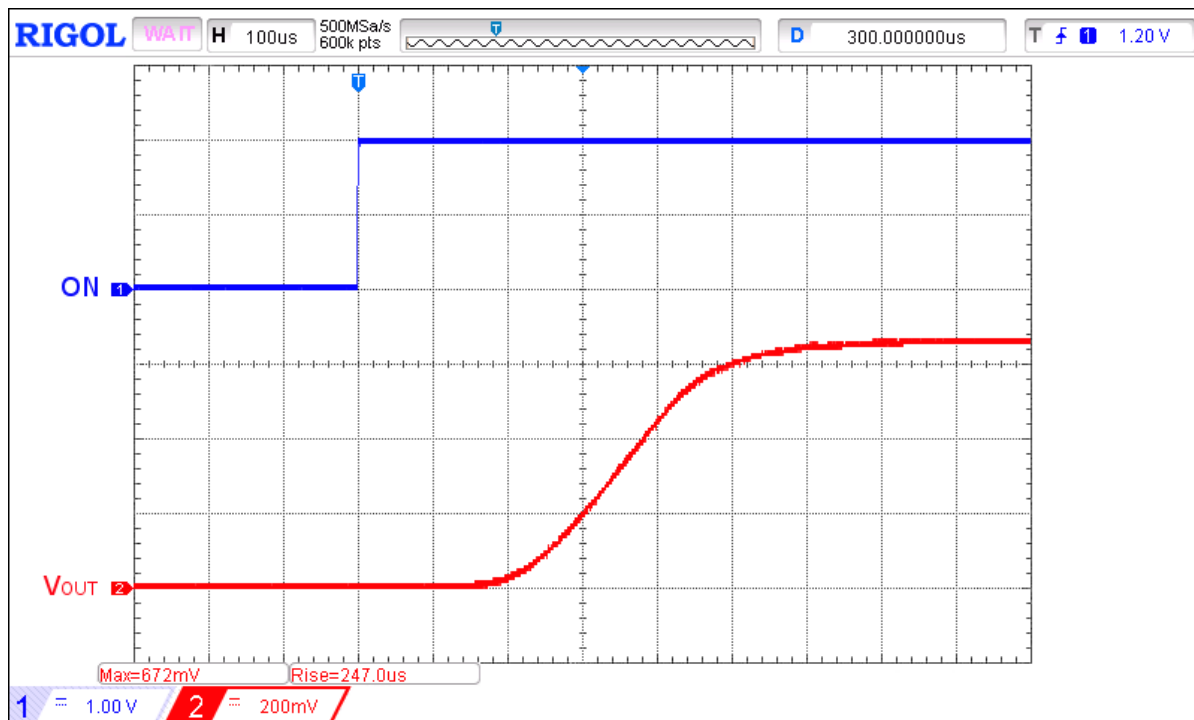


Figure 5: Turn on Operation Waveform for VIN = 0.8 V, CLOAD = 0.1 μF, RLOAD = 0.4 Ω

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**Extending the SLG59M1693C's Maximum Operating Current Range****5 Conclusions**

Using SLG59M1693Cs in parallel lowers the overall  $R_{DS(on)}$ , but current consumption when *on* still remains low. The difference in path length from the voltage source to the IPSs pads may create a current imbalance, so the recommended PCB layout is presented.

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**Extending the SLG59M1693C's Maximum Operating Current Range****Revision History**

<b>Revision</b>	<b>Date</b>	<b>Description</b>
1.0	22-Mar-2018	Initial Version



## Extending the SLG59M1693C's Maximum Operating Current Range

### Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
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