5 Tips for Creating a Custom ASIC

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Much has been written about the advantages of custom ASICs over recent years. In particular, as the growth in the Industrial Internet of Things (IIoT) takes hold, more and more OEMs are looking to develop custom ASICs in order to generate a product that is specific and optimized to their exacting requirements. Due to the non-homogenous nature of IIoT requirements, OEMs who choose to use off-the-shelf standard parts may end up disadvantaging themselves by paying excessively for overly specified, non-optimized chips. Put simply, one-size does not fit all in the IIoT!
Custom ASICs can help OEMs significantly cut the cost of overly specified products and streamline bill of materials management. As more and more companies take this route for their designs, here are some key tips to consider when navigating the custom ASIC path.

1. Work with a supplier that has industry experience.

You have an internal design team which is not fully utilized. That team can develop a custom chip for your next project, right? Not necessarily. Developing a custom chip takes a lot of expertise and know-how, both in design and manufacturing. Successful ASIC companies have been working exclusively in this space for many years. They have teams of analog, digital and RF engineers who have deep experience in the integration of these blocks so that the required performance can be achieved without trade-offs on size, power or cost. These teams are skilled at dealing with any design or layout challenges while adhering to the overall requirements of the chip. They understand the potential impacts of system-level noise, power budgeting and connectivity. Experienced ASIC houses are also adept at leveraging existing silicon-proven IP libraries, which greatly reduces design time. Working with a supplier that has a large portfolio of IP offers many advantages. Having the building blocks internally available means time can be saved as the individual IP and blocks are already proven on silicon. Costs can be reduced also as you are not having to look externally to license all of the blocks. Having this IP knowledge can also include the ability to port IP from one technology node to another when required. This, together with the expertise to leverage and manage their semiconductor foundry, packaging and test supply chains, are critical factors to ensuring success.

2. Choose a partner with access to a broad range of tier-1 suppliers.

To have a successful project, you need to be able to utilize the best suppliers, and you want to have choice of suppliers to ensure a fit for your specific design needs. Achieving the best for your design means that you want to have access to the process node that makes sense for that design. Developing your custom chip firstly means having access to the required tools and IP and then having the ability to manufacture the chip on the process node that makes sense (or having the ability to port the IP being used to the optimal node). After manufacturing, you want to be able to choose the correct package for your product and therefore have a partner that has access to suppliers of many different types of package options. Finally, you want to have this product qualified and tested to guarantee performance and reliability and of course future supply. By choosing the right ASIC partner who has a broad range of these relationships across EDA companies, foundries, package providers and others in the supply chain can help OEMs to have the widest array of choices for their specific design.

3. Think of the future

Is there potential for a future product that may not yet be fully defined, but which might benefit from the work that is being done now? Could you easily add some features to this custom ASIC that would allow you to use this chip across a number of different products both today and in the future? Taking a holistic view of the discovery process will only benefit you.
An example of such a typical custom ASIC engagement where the customer wanted to optimize their BOM and be able to build in some future proofing to their design. A review of their portfolio and roadmap fed into the development of a custom chip that met their performance, size and cost requirements – and left room for future expansion. This included adding more processing power and memory to the chip. While not needed immediately, the additional logic did not impact the final size or cost of the chip and provides future headroom. This was not something that could easily have been implemented using off the shelf standard products. The right partner will help review your product roadmap to see if this is possible, and assess if it makes sense – from cost, size and power perspectives – to implement today.

4. Consolidate what makes sense.

So, with a custom chip, I can consolidate everything that is on my board into a single chip… right?
Well yes, in theory you can. But be sure to consider whether you should do this in all cases. Does it make sense to increase the size of your design by adding extra components that are inexpensive to source? For example, you have a requirement for a large bank of memory. If you integrate all this memory into the custom ASIC it will greatly increase the size of your die and thus increase the cost of your chip. Doing the math, you realize that the memory you need is inexpensive and can be purchased as one single chip. The best option therefore is to keep the memory off chip.
Additionally, you may want to consider your overall power budget. Does adding more to the chip increase the power unnecessarily? Or does having a separate chip and driving signals between the chips end up costing more in terms of power? Or does the off-chip RAM in a much smaller geometry save power overall? Does adding more to the chip increase the power unnecessarily?
What if you have that component that is only available on a particular process technology at a particular node? Even if all the analog and digital circuitry is available on this node, you need to consider whether it make sense to have knock on effects on overall size, performance or cost just to keep it all on the same node and have it all integrated. The alternative would be to design your analog and digital circuitry on the most optimum node and keep that other component separate. Working with an ASIC design authority will help you to understand these trade-offs and only integrate what makes sense for your design and your budget.

5. Lock down your requirements as soon as possible.

The initial planning phase of a custom ASIC is extremely important. Time spent up-front locking down the requirements and then working with the ASIC authority to translate these requirements into the ASIC specifications is vital to ensuring success. You may want to add in some flexibility in order to get as much as you possibly can from a chip. This can be a good idea if you understand these requirements well and adding this flexibility is offering some future proofing to your design.
What you don’t want to do is add in so much flexibility to the design that you negatively impact your time to market, increase your costs and ultimately have a product that is not refined to the original overarching requirements of the chip. Specification feature ‘creep’ in ASIC developments can be costly both in time and resources, and a good ASIC partner will help you weigh the requirements up in the discovery process and have the design locked down.