Adesto Technologies

AT25DF041A & AT25SF041

Comparison

Adesto Field Application
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AT25DF041A and AT25SF041 - comparison

AT25DF041A

- **Single 2.3V - 3.6V or 2.7V - 3.6V Supply**
- **Serial Peripheral Interface (SPI) Compatible**
  - **Supports SPI Modes 0 and 3**
- **70 MHz Maximum Clock Frequency**
- **Flexible, Uniform Erase Architecture**
  - **4-Kbyte Blocks**
  - **32-Kbyte Blocks**
  - **64-Kbyte Blocks**
  - **Full Chip Erase**
- **Individual Sector Protection with Global Protect/Unprotect Feature**
  - **One 16-Kbyte Top Sector**
  - **Two 8-Kbyte Sectors**
  - **One 32-Kbyte Sector**
  - **Seven 64-Kbyte Sectors**
- **Hardware Controlled Locking of Protected Sectors via $\overline{\text{WP}}$ pin**
- **Flexible Programming Options**
  - **Byte/Page Program (1 to 256 Bytes)**
  - **Sequential Program Mode Capability**
- **Fast Program and Erase Times**
  - **1.2 ms Typical Page Program (256 Bytes) Time**
  - **50 ms Typical 4-Kbyte Block Erase Time**
  - **250 ms Typical 32-Kbyte Block Erase Time**
  - **400 ms Typical 64-Kbyte Block Erase Time**
- **Automatic Checking and Reporting of Erase/Program Failures**
- **JEDEC Standard Manufacturer and Device ID Read Methodology**
- **Low Power Dissipation**
  - **5 mA Active Read Current (Typical)**
  - **15 µA Deep Power-down Current (Typical)**
- **Endurance: 100,000 Program/Erase Cycles**
- **Data Retention: 20 Years**

AT25SF041

- Single 2.5V - 3.6V Supply → New
- Serial Peripheral Interface (SPI) Compatible
  - Supports SPI Modes 0 and 3
  - Supports Dual and Quad Output Read → New
- 104MHz Maximum Operating Frequency → New
  - Clock-to-Output (t_V) of 6 ns
- Flexible, Optimized Erase Architecture for Code + Data Storage Applications
  - Uniform 4-Kbyte Block Erase
  - Uniform 32-Kbyte Block Erase
  - Uniform 64-Kbyte Block Erase
- Full Chip Erase
- Hardware Controlled Locking of Protected Blocks via $\overline{\text{WP}}$ Pin → New
- 3 Protected Programmable Security Register Pages → New
- Flexible Programming
  - Byte/Page Program (1 to 256 Bytes)
- Fast Program and Erase Times
  - 0.7ms Typical Page Program (256 Bytes) Time → New
  - 70ms Typical 4-Kbyte Block Erase Time
  - 300ms Typical 32-Kbyte Block Erase Time
  - 600ms Typical 64-Kbyte Block Erase Time
- JEDEC Standard Manufacturer and Device ID Read Methodology
- Low Power Dissipation
  - 2µA Deep Power-Down Current (Typical) → New
  - 10µA Standby current (Typical)
  - 4mA Active Read Current (Typical) → Improved
- Endurance: 100,000 Program/Erase Cycles
- Data Retention: 20 Years

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AT25DF041A vs AT25SF041 Command Set

Command	AT25DF041A	AT25SF041
Vcc	2.7V - 3.6V 2.3V - 3.6V	2.5V - 3.6V
Read Array	0Bh	0Bh
Read Array	03h	03h
Block Erase, 4KB	20h	20h
Block Erase, 32KB	52h	52h
Block Erase, 64KB	D8h	D8h
Chip Erase	60h	60h
Chip Erase	C7h	C7h
Byte/Page Program	02h	02h
Sequential Programing	ADh	
Sequential Programing	AFh	
Write Enable	06h	06h
Write Disable	04h	04h
Protect Sector	36h	
Unprotect Sector	39h	
Global Protect/Unprotect	Use Write Status Register Command	
Read Sector Protection Register	3Ch	
Read Status Register, Byte 1	05h	05h
Write Status Register Byte 1	01h	01h
Read Manufacturer and Device ID	9Fh	9Fh
Deep Power-Down	B9h	B9h
Resume from Deep Power-Down and Read ID	ABh	ABh

Need Software change

Program, Erase Time, and Packages

Command	AT25DF041A	AT25SF041
Vcc	2.7V - 3.6V 2.3V - 3.6V	2.5V - 3.6V
Page Program Time	5msec max	2.5 msec Max
Block Erase, 4KB	200msec max	300 msec Max
Block Erase, 32KB	600msec max	1300 msec Max
Block Erase, 64KB	950msec max	2.2 sec Max
Chip Erase	7 sec max	10 sec Max
Manufacture and Product ID	1F 44 01 00	1F 84 01
Status Register	1 bytes	2 bytes
MH (5x6x0.6mm)	MH	MH
SSH, SSU	SSH	SSH
SH, SU	SH	SH
MAH (2x3x0.6mm)		MAH

Need Software change

Block Erase Time:

- If S/W uses a fixed Timeout for End of Program / Erase cycles:
  - delay period may need to be extended to allow for the increased spec
- If S/W polls the device for End of Program / Erase cycles:
  - These spec changes should be transparent in the system

AT25DF041A to AT25SF041 Migration

The following items require software changes

Sector Protection:

- AT25DF041A – Sector Protection
- AT25SF041 – Block Protection via WP and Status register

Sequential programming:

- AT25SF041 does not support command ADh, AFh

Device ID:

- Refer to page 4.

Status Register:

- Bit 0 (Rdy/Busy) and bit 1(WEL) are the same.
- Other bits are different, please refer to datasheet.

Block Erase Time:

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  - delay period may need to be extended to allow for the increased spec
- If S/W polls the device for End of Program / Erase cycles:
  - These spec changes should be transparent in the system